Practitioner's Docket No. 104 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of

Inventor(s): Ted A. Loxley

WARNING: *37 C.F.R. § 1.41(a)(1) points out:*

"(a) A patent is applied for in the name or names of the actual inventor or inventors.

"(1) The inventorship of a nonprovisional application is that inventorship set forth in the oath or declaration as prescribed by § 1.63, except as provided for in § 1.53(d)(4) and § 1.63(d). If an oath or declaration as prescribed by § 1.63 is not filed during the pendency of a nonprovisional application, the inventorship is that inventorship set forth in the application papers filed pursuant to § 1.53(b), unless a petition under this paragraph accompanied by the fee set forth in § 1.17(i) is filed supplying or changing the name or names of the inventor or inventors."

For (title):

Process and Apparatus for Cleaning Silicon Wafers

CERTIFICATION UNDER 37 C.F.R. 1.10*
(Express Mail label number is mandatory.)
(Express Mail certification is optional.)

I hereby certify that this New Application Transmittal and the documents referred to as attached therein are being deposited with the United States Postal Service on this date January 22, 2000, in an envelope as "Express Mail Post Office to Addressee," mailing Label Number EK216390975, addressed to the: Assistant Commissioner for Patents, Washington, D.C. 20231.

Vincent A. Greene

(type or print name of person mailing paper)

Vincent A Greene

Signature of person mailing paper

WARNING: *Certificate of mailing (first class) or facsimile transmission procedures of 37 C.F.R. 1.8 cannot be used to obtain a date of mailing or transmission for this correspondence.*

"WARNING: *Each paper or fee filed by "Express Mail" **must** have the number of the "Express Mail" mailing label placed thereon prior to mailing. 37 C.F.R. 1.10(b).*
*"Since the filing of correspondence under § 1.10 without the Express Mail mailing label thereon is an oversight that can be avoided by the exercise of reasonable care, requests for waiver of this requirement will **not** be granted on petition." Notice of Oct. 24, 1996, 60 Fed. Reg. 56,439, at 56,442.*

1. Type of Application

This new application is for a(n)

(check one applicable item below)

- [x] Original (nonprovisional)
- [ ] Design
- [ ] Plant

WARNING: *Do not use this transmittal for a completion in the U.S. of an International Application under 35 U.S.C. 371(c)(4), unless the International Application is being filed as a divisional, continuation or continuation-in-part application.*

WARNING: *Do not use this transmittal for the filing of a provisional application.*

NOTE: If one of the following 3 items apply, then complete and attach ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF A PRIOR U.S. APPLICATION CLAIMED and a NOTIFICATION IN PARENT APPLICATION OF THE FILING OF THIS CONTINUATION APPLICATION.

- [ ] Divisional.
- [ ] Continuation.
- [ ] Continuation-in-part (C-I-P).

2. Benefit of Prior U.S. Application(s) (35 U.S.C. 119(e), 120, or 121)

NOTE: A nonprovisional application may claim an invention disclosed in one or more prior filed copending nonprovisional applications or copending international applications designating the United States of America. In order for a nonprovisional application to claim the benefit of a prior filed copending nonprovisional application or copending international application designating the United States of America, each prior application must name as an inventor at least one inventor named in the later filed nonprovisional application and disclose the named inventor's invention claimed in at least one claim of the later filed nonprovisional application in the manner provided by the first paragraph of 35 U.S.C. 112. Each prior application must also be:

(i) An international application entitled to a filing date in accordance with PCT Article 11 and designating the United States of America; or

(ii) Complete as set forth in § 1.51(b); or

(iii) Entitled to a filing date as set forth in § 1.53(b) or § 1.53(d) and include the basic filing fee set forth in § 1.16; or

(iv) Entitled to a filing date as set forth in § 1.53(b) and have paid therein the processing and retention fee set forth in § 1.21(l) within the time period set forth in § 1.53(f).

37 C.F.R. § 1.78(a)(1).

NOTE: If the new application being transmitted is a divisional, continuation or a continuation-in-part of a parent case, or where the parent case is an International Application which designated the U.S., or benefit of a prior provisional application is claimed, then check the following item and complete and attach ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

WARNING: *If an application claims the benefit of the filing date of an earlier filed application under 35 U.S.C. 120, 121 or 365(c), the 20-year term of that application will be based upon the filing date of the earliest U.S. application that the application makes reference to under 35 U.S.C. 120, 121 or 365(c). (35 U.S.C. 154(a)(2) does not take into account, for the determination of the patent term, any application on which priority is claimed under 35 U.S.C. 119, 365(a) or 365(b).) For a C-I-P application, applicant should review whether any claim in the patent that will issue is supported by an earlier application and, if not, the applicant should consider canceling the reference to the earlier filed application. The term of a patent is not based on a claim-by-claim approach. See Notice of April 14, 1995, 60 Fed. Reg. 20,195, at 20,205.*

WARNING: *When the last day of pendency of a provisional application falls on a Saturday, Sunday, or Federal holiday within the District of Columbia, any nonprovisional application claiming benefit of the provisional application must be filed prior to the Saturday, Sunday, or Federal holiday within the District of Columbia. See 37 C.F.R. § 1.78(a)(3).*

☐ The new application being transmitted claims the benefit of prior U.S. application(s). Enclosed are ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

3. Papers Enclosed

A. Required for filing date under 37 C.F.R. § 1.53(b) (Regular) or 37 C.F.R. § 1.153 (Design) Application

60 Pages of specification

8 Pages of claims

2 Sheets of drawing

WARNING: ***DO NOT*** *submit original drawings. A high quality copy of the drawings should be supplied when filing a patent application. The drawings that are submitted to the Office must be on strong, white, smooth, and non-shiny paper and meet the standards according to § 1.84. If corrections to the drawings are necessary, they should be made to the original drawing and a high-quality copy of the corrected original drawing then submitted to the Office. Only one copy is required or desired. For comments on proposed then-new 37 CFR 1.84, see Notice of March 9, 1988 (1990 O.G. 57-62).*

NOTE: "Identifying indicia, if provided, should include the application number or the title of the invention, inventor's name, docket number (if any), and the name and telephone number of a person to call if the Office is unable to match the drawings to the proper application. This information should be placed on the back of each sheet of drawing a minimum distance of 1.5 cm. (5/8 inch) down from the top of the page . . ." 37 C.F.R. 1.84(c)).

(complete the following, if applicable)

☐ The enclosed drawing(s) are photograph(s), and there is also attached a "PETITION TO ACCEPT PHOTOGRAPH(S) AS DRAWING(S)." 37 C.F.R. 1.84(b).

☐ formal

☒ informal

B. Other Papers Enclosed

7 Pages of declaration and power of attorney

1 Pages of abstract

____ Other

4. Additional papers enclosed

☐ Amendment to claims

☐ Cancel in this applications claims _____ before calculating the filing fee. (At least one original independent claim must be retained for filing purposes.)

☐ Add the claims shown on the attached amendment. (Claims added have been numbered consecutively following the highest numbered original claims.)

☐ Preliminary Amendment

☐ Information Disclosure Statement (37 C.F.R. 1.98)

☐ Form PTO–1449 (PTO/SB/08A and 08B)

☐ Citations

☐ Declaration of Biological Deposit

☐ Submission of "Sequence Listing," computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleotide and/or amino acid sequence.

☐ Authorization of Attorney(s) to Accept and Follow Instructions from Representative

☐ Special Comments

☐ Other

5. Declaration or oath (including power of attorney)

NOTE: A newly executed declaration is not required in a continuation or divisional application provided that the prior nonprovisional application contained a declaration as required, the application being filed is by all or fewer than all the inventors named in the prior application, there is no new matter in the application being filed, and a copy of the executed declaration filed in the prior application (showing the signature or an indication thereon that it was signed) is submitted. The copy must be accompanied by a statement requesting deletion of the names of person(s) who are not inventors of the application being filed. If the declaration in the prior application was filed under § 1.47, then a copy of that declaration must be filed accompanied by a copy of the decision granting § 1.47 status or, if a nonsigning person under § 1.47 has subsequently joined in a prior application, then a copy of the subsequently executed declaration must be filed. See 37 C.F.R. §§ 1.63(d)(1)–(3).

NOTE: A declaration filed to complete an application must be executed, identify the specification to which it is directed, identify each inventor by full name including family name and at least one given name, without abbreviation together with any other given name or initial, and the residence, post office address and country or citizenship of each inventor, and state whether the inventor is a sole or joint inventor. 37 C.F.R. § 1.63(a)(1)–(4).

☒ Enclosed

Executed by Ted A .Loxley

(check **all** *applicable boxes)*

☒ inventor(s).

☐ legal representative of inventor(s). 37 CFR 1.42 or 1.43.

☐ joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached.

☐ This is the petition required by 37 CFR 1.47 and the statement required by 37 CFR 1.47 is also attached. See item 13 below for fee.

☐ Not Enclosed.

NOTE: Where the filing is a completion in the U.S. of an International Application or where the completion of the U.S. application contains subject matter in addition to the International Application, the application may be treated as a continuation or continuation-in-part, as the case may be, utilizing ADDED PAGE FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION CLAIMED.

☐ Application is made by a person authorized under 37 C.F.R. 1.41(c) on behalf of *all* the above named inventor(s).

(The declaration or oath, along with the surcharge required by 37 CFR 1.16(e) can be filed subsequently).

☐ Showing that the filing is authorized. *(not required unless called into question. 37 CFR 1.41(d))*

6. Inventorship Statement

WARNING: *If the named inventors are each not the inventors of all the claims an explanation, including the ownership of the various claims at the time the last claimed invention was made, should be submitted.*

The inventorship for all the claims in this application are:

☒ The same.

or

☐ Not the same. An explanation, including the ownership of the various claims at the time the last claimed invention was made,

- ☐ is submitted.
- ☐ will be submitted.

7. Language

NOTE: An application including a signed oath or declaration may be filed in a language other than English. An English translation of the non-English language application and the processing fee of $130.00 required by 37 CFR 1.17(k) is required to be filed with the application, or within such time as may be set by the Office. 37 CFR 1.52(d).

☒ English

☐ Non-English

- ☐ The attached translation includes a statement that the translation is accurate. 37 C.F.R. 1.52(d).

8. Assignment

☐ An assignment of the invention to _____

_____

- ☐ is attached. A separate ☐ "COVER SHEET FOR ASSIGNMENT (DOCUMENT) ACCOMPANYING NEW PATENT APPLICATION" or ☐ FORM PTO 1595 is also attached.
- ☐ will follow.

NOTE: "If an assignment is submitted with a new application, send two separate letters-one for the application and one for the assignment." Notice of May 4, 1990 (1114 O.G. 77-78).

WARNING: *A newly executed "CERTIFICATE UNDER 37 CFR 3.73(b)" must be filed when a continuation-in-part application is filed by an assignee. Notice of April 30, 1993, 1150 O.G. 62-64.*

9. Certified Copy

Certified copy(ies) of application(s)

Country	Appln. No.	Filed
Country	Appln. No.	Filed
Country	Appln. No.	Filed

from which priority is claimed

☐ is (are) attached.

☐ will follow.

NOTE: The foreign application forming the basis for the claim for priority must be referred to in the oath or declaration. 37 CFR 1.55(a) and 1.63.

NOTE: This item is for any foreign priority for which the application being filed directly relates. If any parent U.S. application or International Application from which this application claims benefit under 35 U.S.C. 120 is itself entitled to priority from a prior foreign application, then complete item 18 on the ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

10. Fee Calculation (37 C.F.R. 1.16)

A. ☒ Regular application

CLAIMS AS FILED					
	Number filed	Number Extra		Rate	Basic Fee 37 C.F.R. 1.16(a) $690.00
Total Claims (37 CFR 1.16(c))	30 – 20 =	10	×	$18.00	$180.00
Independent Claims (37 CFR 1.16(b))	8 – 3 =	5	×	$78.00	$390.00
Multiple dependent claim(s), if any (37 CFR 1.16(d))			+	$270.00	

☐ Amendment cancelling extra claims is enclosed.

☐ Amendment deleting multiple-dependencies is enclosed.

☐ Fee for extra claims is not being paid at this time.

NOTE: If the fees for extra claims are not paid on filing they must be paid or the claims cancelled by amendment, prior to the expiration of the time period set for response by the Patent and Trademark Office in any notice of fee deficiency. 37 CFR 1.16(d).

Filing Fee Calculation $1,260.00

B. ☐ Design application ($330.00—37 CFR 1.16(f))

Filing Fee Calculation $_____

C. ☐ Plant application ($540.00—37 CFR 1.16(g))

Filing fee calculation $_____

11. Small Entity Statement(s)

☒ Statement(s) that this is a filing by a small entity under 37 CFR 1.9 and 1.27 is (are) attached.

WARNING: *"Status as a small entity must be specifically established in each application or patent in which the status is available and desired. Status as a small entity in one application or patent does not affect any other application or patent, including applications or patents which are directly or indirectly dependent upon the application or patent in which the status has been established. The refiling of an application under § 1.53 as a continuation, division, or continuation-in-part (including a continued prosecution application under § 1.53(d)), or the filing of a reissue application requires a new determination as to continued entitlement to small entity status for the continuing or reissue application. A nonprovisional application claiming benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) of a prior application, or a reissue application may rely on a statement filed in the prior application or in the patent if the nonprovisional application or the reissue application includes a reference to the statement in the prior application or in the patent or includes a copy of the statement in the prior application or in the patent and status as a small entity is still proper and desired. The payment of the small entity basic statutory filing fee will be treated as such a reference for purposes of this section." 37 C.F.R. § 1.28(a)(2).*

(complete the following, if applicable)

☐ Status as a small entity was claimed in prior application

_____ / _____, filed on _____, from which benefit is being claimed for this application under:

35 U.S.C. ☐ 119(e),
☐ 120,
☐ 121,
☐ 365(c),

and which status as a small entity is still proper and desired.

☐ A copy of the statement in the prior application is included.

Filing Fee Calculation (50% of **A**, **B** or **C** above)

$630.00

NOTE: Any excess of the full fee paid will be refunded if small entitiy status is established and a refund request are filed within 2 months of the date of timely payment of a full fee. The two-month period is not extendable under § 1.136. 37 CFR 1.28(a).

12. Request for International-Type Search (37 C.F.R. 1.104(d))

(complete, if applicable)

☐ Please prepare an international-type search report for this application at the time when national examination on the merits takes place.

13. Fee Payment Being Made at This Time

☐ Not Enclosed

☐ No filing fee is to be paid at this time.
(This and the surcharge required by 37 C.F.R. 1.16(e) can be paid subsequently.)

☒ Enclosed

☒ Filing fee	$630.00
☐ Recording assignment ($40.00; 37 C.F.R. 1.21(h)) (See attached "COVER SHEET FOR ASSIGNMENT ACCOMPANYING NEW APPLICATION".)	$ _____
☐ Petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached ($130.00; 37 C.F.R. 1.47 and 1.17(i))	$ _____
☐ For processing an application with a specification in a non-English language ($130.00; 37 C.F.R. 1.52(d) and 1.17(k))	$ _____
☐ Processing and retention fee ($130.00; 37 C.F.R. 1.53(d) and 1.21(l))	$ _____
☐ Fee for international-type search report ($40.00; 37 C.F.R. 1.21(e))	$ _____

NOTE: 37 CFR 1.21(l) establishes a fee for processing and retaining any application that is abandoned for failing to complete the application pursuant to 37 CFR 1.53(f) and this, as well as the changes to 37 CFR 1.53 and 1.78(a)(1), indicate that in order to obtain the benefit of a prior U.S. application, either the basic filing fee must be paid, or the processing and retention fee of § 1.21(l) must be paid, within 1 year from notification under § 53(f).

Total fees enclosed $630.00

14. Method of Payment of Fees

☒ Check in the amount of $630.00

☐ Charge Account No. _____ in the amount of $_____

A duplicate of this transmittal is attached.

NOTE: Fees should be itemized in such a manner that it is clear for which purpose the fees are paid. 37 CFR 1.22(b).

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15. Authorization to Charge Additional Fees

WARNING: *If no fees are to be paid on filing, the following items should not be completed.*

WARNING: *Accurately count claims, especially multiple dependent claims, to avoid unexpected high charges, if extra claim charges are authorized.*

☐ The Commissioner is hereby authorized to charge the following additional fees by this paper and during the entire pendency of this application to Account No. _____:

- ☐ 37 C.F.R. 1.16(a), (f) or (g) (filing fees)
- ☐ 37 C.F.R. 1.16(b), (c) and (d) (presentation of extra claims)

NOTE: Because additional fees for excess or multiple dependent claims not paid on filing or on later presentation must only be paid or these claims cancelled by amendment prior to the expiration of the time period set for response by the PTO in any notice of fee deficiency (37 CFR 1.16(d)), it might be best not to authorize the PTO to charge additional claim fees, except possibly when dealing with amendments after final action.

- ☐ 37 C.F.R. 1.16(e) (surcharge for filing the basic filing fee and/or declaration on a date later than the filing date of the application)
- ☐ 37 C.F.R. §§ 1.17(a)(1)–(5) (extension fees pursuant to § 1.136(a)).
- ☐ 37 C.F.R. 1.17 (application processing fees)

NOTE: ". . .A written request may be submitted in an application that is an authorization to treat any concurrent or future reply, requiring a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. An authorization to charge all required fees, fees under § 1.17, or all required extension of time fees will be treated as a constructive petition for an extension of time in any concurrent or future reply requiring a petition for an extension of time under this paragraph for its timely submission. Submission of the fee set forth in § 1.17(a) will also be treated as a constructive petition for an extension of time in any concurrent reply requiring a petition for an extension of time under this paragraph for its timely submission." 37 C.F.R. § 1.136(a)(3).

- ☐ 37 C.F.R. 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 C.F.R. 1.311(b))

NOTE: Where an authorization to charge the issue fee to a deposit account has been filed before the mailing of a Notice of Allowance, the issue fee will be automatically charged to the deposit account at the time of mailing the notice of allowance. 37 CFR 1.311(b).

NOTE: 37 CFR 1.28(b) requires "Notification of any change in status resulting in loss of entitlement to small entity status must be filed in the application . . . prior to paying, or at the time of paying, . . . the issue fee. . . ." From the wording of 37 CFR 1.28(b), (a) notification of change of status must be made even if the fee is paid as "other than a small entity" and (b) no notification is required if the change is to another small entity.

16. Instructions as to Overpayment

NOTE: ". . . Amounts of twenty-five dollars or less will not be returned unless specifically requested within a reasonable time, nor will the payer be notified of such amounts; amounts over twenty-five dollars may be returned by check or, if requested, by credit to a deposit account." 37 C.F.R. § 1.26(a).

☐ Credit Account No. _____

☒ Refund

Vincent A Greene

SIGNATURE OF PRACTITIONER

Reg. No. 17,389

Vincent A. Greene

(type or print name of attorney)

Tel. No. (216) 481-7772

25931 Euclid Avenue, Suite 116

P.O. Address

Customer No.

Cleveland, Ohio 44132

16390975

☐ **Incorporation by reference of added pages**

(check the following item if the application in this transmittal claims the benefit of prior U.S. application(s) (including an international application entering the U.S. stage as a continuation, divisional or C-I-P application) and complete and attach the ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED)

☒ Plus Added Pages for New Application Transmittal Where Benefit of Prior U.S. Application(s) Claimed

Number of pages added 1

☐ Plus Added Pages for Papers Referred to in Item 4 Above

Number of pages added ____

☐ Plus added pages deleting names of inventor(s) named in prior application(s) who is/are no longer inventor(s) of the subject matter claimed in this application.

Number of pages added ____

☐ Plus "Assignment Cover Letter Accompanying New Application"

Number of pages added ____

☐ **Statement Where No Further Pages Added**

(if no further pages form a part of this Transmittal, then end this Transmittal with this page and check the following item)

☐ This transmittal ends with this page.

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ADDED PAGE FOR APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED

NOTE: See 37 CFR 1.78.

17. Relate Back

WARNING: *If an application claims the benefit of the filing date of an earlier filed application under 35 U.S.C. 120, 121 or 365(c), the 20-year term of that application will be based upon the filing date of the earliest U.S. application that the application makes reference to under 35 U.S.C. 120, 121 or 365(c). (35 U.S.C. 154(a)(2) does not take into account, for the determination of the patent term, any application on which priority is claimed under 35 U.S.C. 119, 365(a) or 365(b).) For a c-i-p application, applicant should review whether any claim in the patent that will issue is supported by an earlier application and, if not, the applicant should consider canceling the reference to the earlier filed application. The term of a patent is not based on a claim-by-claim approach. See Notice of April 14, 1995, 60 Fed. Reg. 20,195, at 20,205.*

(complete the following, if applicable)

☐ Amend the specification by inserting, before the first line, the following sentence:

A. 35 U.S.C. 119(e)

NOTE: "Any nonprovisional application claiming the benefit of one or more prior filed copending provisional applications must contain or be amended to contain in the first sentence of the specification following the title a reference to each such prior provisional application, identifying it as a provisional application, and including the provisional application number (consisting of series code and serial number)." 37 C.F.R. § 1.78(a)(4).

☐ "This application claims the benefit of U.S. Provisional Application(s) No(s).:

APPLICATION NO(S).:	FILING DATE
60 / 116,940	January 23, 1999 "
/	"
/	"

(Added Page for Application Transmittal Where Benefit of Prior U.S. Application(s) Claimed

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SPECIFICATION IDENTIFICATION

the specification of which:

(complete (a), (b), or (c))

(a) ☐ is attached hereto.

NOTE: *"The following combinations of information supplied in an oath or declaration filed on the application filing date with a specification are acceptable as minimums for identifying a specification and compliance with any one of the items below will be accepted as complying with the identification requirement of 37 CFR 1.63:*

"(1) name of inventor(s), and reference to an attached specification which is both attached to the oath or declaration at the time of execution and submitted with the oath or declaration on filing;

"(2) name of inventor(s), and attorney docket number which was on the specification as filed; or

"(3) name of inventor(s), and title which was on the specification as filed."

Notice of July 13, 1995 (1177 O.G. 60).

(b) ☐ was filed on _____, as ☐ Serial No. 0 /_____ or ☐ _____ and was amended on _____ *(if applicable).*

NOTE: *Amendments filed after the original papers are deposited with the PTO that contain new matter are not accorded a filing date by being referred to in the declaration. Accordingly, the amendments involved are those filed with the application papers or, in the case of a supplemental declaration, are those amendments claiming matter not encompassed in the original statement of invention or claims. See 37 C.F.R. § 1.67.*

NOTE: *"The following combinations of information supplied in an oath or declaration filed after the filing date are acceptable as minimums for identifying a specification and compliance with any one of the items below will be accepted as complying with the identification requirement of 37 CFR 1.63:*

"(A) application number (consisting of the series code and the serial number, e.g., 08/123,456);

"(B) serial number and filing date;

"(C) attorney docket number which was on the specification as filed;

"(D) title which was on the specification as filed and reference to an attached specification which is both attached to the oath or declaration at the time of execution and submitted with the oath or declaration; or

"(E) title which was on the specification as filed and accompanied by a cover letter accurately identifying the application for which it was intended by either the application number (consisting of the series code and the serial number, e.g., 08/123,456), or serial number and filing date. Absent any statement(s) to the contrary, it will be presumed that the application filed in the PTO is the application which the inventor(s) executed by signing the oath or declaration."

M.P.E.P. § 601.01(a), 7th Ed.

(c) ☐ was described and claimed in PCT International Application No. _____, filed on _____ and as amended under PCT Article 19 on _____ *(if any).*

SUPPLEMENTAL DECLARATION (37 C.F.R. § 1.67(b))

(complete the following where a supplemental declaration is being submitted)

☐ I hereby declare that the subject matter of the

☐ attached amendment

☐ amendment filed on _____

was part of my/our invention and was invented before the filing date of the original application, above-identified, for such invention.

ACKNOWLEDGEMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in 37, Code of Federal Regulations, § 1.56,

(also check the following items, if desired)

☐ and which is material to the examination of this application, namely, information where there is a substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent, and

☐ in compliance with this duty, there is attached an information disclosure statement, in accordance with 37 C.F.R. § 1.98.

PRIORITY CLAIM (35 U.S.C. §§ 119(a)–(d))

NOTE: "The claim to priority need be in no special form and may be made by the attorney or agent if the foreign application is referred to in the oath or declaration as required by § 1.63. The claim for priority and the certified copy of the foreign application specified in 35 U.S.C. 119(b) must be filed in the case of an interference (§ 1.630), when necessary to overcome the date of a reference relied upon by the examiner, when specifically required by the examiner, and in all other situations, before the patent is granted. If the claim for priority or the certified copy of the foreign application is filed after the date the issue fee is paid, it must be accompanied by a petition requesting entry and by the fee set forth in § 1.17(i). If the certified copy is not in the English language, a translation need not be filed except in the case of interference; or when necessary to overcome the date of a reference relied upon by the examiner; or when specifically required by the examiner, in which event an English language translation must be filed together with a statement that the translation of the certified copy is accurate." 37 C.F.R. § 1.55(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §§ 119(a)–(d) of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

(complete (d) or (e))

(d) ☒ no such applications have been filed.

(e) ☐ such applications have been filed as follows.

NOTE: Where item (c) is entered above and the International Application which designated the U.S. itself claimed priority check item (e), enter the details below and make the priority claim.

PRIOR FOREIGN/PCT APPLICATION(S) FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS APPLICATION AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. § 119(a)-(d)

COUNTRY (OR INDICATE IF PCT)	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 37 USC 119
			☐ YES NO ☐
			☐ YES NO ☐
			☐ YES NO ☐
			☐ YES NO ☐
			☐ YES NO ☐

CLAIM FOR BENEFIT OF PRIOR U.S. PROVISIONAL APPLICATION(S)
(34 U.S.C. § 119(e))

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

PROVISIONAL APPLICATION NUMBER	FILING DATE
60/116,940	January 23, 1999

CLAIM FOR BENEFIT OF EARLIER US/PCT APPLICATION(S) UNDER 35 U.S.C. § 120

☐ The claim for the benefit of any such applications are set forth in the attached ADDED PAGES TO COMBINED DECLARATION AND POWER OF ATTORNEY FOR DIVISIONAL, CONTINUATION OR CONTINUATION-IN PART (C-I-P) APPLICATION.

16390975

ALL FOREIGN APPLICATION(S), *IF ANY*, FILED MORE THAN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

_____

_____

_____

NOTE: If the application filed more than 12 months from the filing date of this application is a PCT filing forming the basis for this application entering the United States as (1) the national stage, or (2) a continuation, divisional, or continuation-in-part, then also complete ADDED PAGES TO COMBINED DECLARATION AND POWER OF ATTORNEY FOR DIVISIONAL, CONTINUATION OR C-I-P APPLICATION for benefit of the prior U.S. or PCT application(s) under 35 U.S.C. § 120.

POWER OF ATTORNEY

I hereby appoint the following practitioner(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

(list name and registration number)

Vincent A. Greene

Registration No. 17,389

(check the following item, if applicable)

☐ I hereby appoint the practitioner(s) associated with the Customer Number provided below to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

☐ Attached, as part of this declaration and power of attorney, is the authorization of the above-named practitioner(s) to accept and follow instructions from my representative(s).

SEND CORRESPONDENCE TO

DIRECT TELEPHONE CALLS TO:
(Name and telephone number)

☒ Address Vincent A. Greene

25931 Euclid Avenue, Suite 116

Cleveland, Ohio 44132

☐ Customer Number _____

16390975

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE(S)

NOTE: Carefully indicate the family (or last) name, as it should appear on the filing receipt and all other documents.

NOTE: Each inventor must be identified by full name, including the family name, and at least one given name without abbreviation together with any other given name or initial, and by his/her residence, post office address and country of citizenship. 37 CFR § 1.63(a)(3).

NOTE: Inventors may execute separate declarations/oaths provided each declaration/oath sets forth all the inventors. Section 1.63(a)(3) requires that a declaration/oath, inter alia, identify each inventor and prohibits the execution of separate declarations/oaths which each sets forth only the name of the executing inventor. 62 Fed. Reg. 53,131, 53,142, October 10, 1997,

Full name of sole or first inventor

TED (GIVEN NAME) A. (MIDDLE INITIAL OR NAME) LOXLEY (FAMILY (OR LAST NAME))

Inventor's signature Ted A. Loxley

Date 1-21-2000 **Country of Citizenship** U.S.A.

Residence 236 Tom Corwin Road, Wellston, Ohio 45692

Post Office Address 236 Tom Corwin Road, Wellston, Ohio 45692

Full name of second joint inventor, if any

(GIVEN NAME) (MIDDLE INITIAL OR NAME) (FAMILY (OR LAST NAME))

Inventor's signature _____

Date _____ **Country of Citizenship** _____

Residence _____

Post Office Address _____

Full name of third joint inventor, if any

(GIVEN NAME) (MIDDLE INITIAL OR NAME) (FAMILY (OR LAST NAME))

Inventor's signature _____

Date _____ **Country of Citizenship** _____

Residence _____

Post Office Address _____

(check proper box(es) for any of the following added page(s) that form a part of this declaration)

☐ **Signature** for fourth and subsequent joint inventors. *Number of pages added* _____.

* * *

☐ **Signature** by administrator(trix), executor(trix) or legal representative for deceased or incapacitated inventor. *Number of pages added* _____.

* * *

☐ **Signature** for inventor who refuses to sign or cannot be reached by person authorized under 37 CFR 1.47. *Number of pages added* _____

* * *

☐ Added page for **signature** by one joint inventor on behalf of deceased inventor(s) where legal representative cannot be appointed in time. (37 CFR 1.47)

* * *

☐ Added pages to combined declaration and power of attorney for divisional, continuation, or continuation-in-part (C-I-P) application.

☐ Number of pages added _____

* * *

☐ Authorization of practitioner(s) to accept and follow instructions from representative.

* * *

(if no further pages form a part of this Declaration, then end this Declaration with this page and check the following item)

☒ This declaration ends with this page.

Practitioner's Docket No. 104 **PATENT**

- ☐ Applicant Ted A. Loxley
- ☐ Application No.
- ☐ Filed on Jan. 2000
- ☐ Patentee
- ☐ Patent No.
- ☐ Issued on

Title: Process and Apparatus for Cleaning Silicon Wafers

STATEMENT CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) and 1.27(b))—INDEPENDENT INVENTOR

As a below named inventor, I hereby state that I qualify as an independent inventor, as defined in 37 CFR 1.9(c), for purposes of paying reduced fees to the United States Patent and Trademark Office under Sections 41(a) and (b) of Title 35, United States Code, to the Patent and Trademark Office, with regard to the invention described in

- ☒ the specification filed herewith, with title as listed above.
- ☐ the application identified above.
- ☐ the patent identified above.

I have not assigned, granted, conveyed or licensed, and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who would not qualify as an independent inventor under 37 CFR 1.9(c), if that person had made the invention, or to any concern that would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

- ☐ No such person, concern, or organization exists.
- ☐ Each such person, concern or organization is listed below.*

**NOTE: Separate statements are required from each named person, concern or organization having rights to the invention as to their status as small entities. (37 CFR 1.27)*

FULL NAME ______________________

ADDRESS ______________________

☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

FULL NAME ______________________

ADDRESS ______________________

☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

FULL NAME ______________________

ADDRESS ______________________

☐ INDIVIDUAL ☐ SMALL BUSINESS CONCERN ☐ NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

(check the following item, if desired)

NOTE: The following verification statement need not be made in accordance with the rules published on Oct. 10, 1997, 62 Fed. Reg. 52131, effective Dec. 1, 1997.

NOTE: "The presentation to the Office (whether by signing, filing, submitting, or later advocating) of any paper by a party, whether a practitioner or non-practitioner, constitutes a certification under § 10.18(b) of this chapter. Violations of § 10.18(b)(2) of this chapter by a party, whether a practitioner or non-practitioner, may result in the imposition of sanctions under § 10.18(c) of this chapter. Any practitioner violating § 10.18(b) may also be subject to disciplinary action. See §§ 10.18(d) and 10.23(c)(15)." 37 C.F.R. § 1.4(d)(2).

☐ I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Ted A. Loxley

Name of inventor

Ted A. Loxley

Signature of Inventor

Date 1-21-2000

Name of inventor

Signature of Inventor

Date

Name of inventor

Signature of Inventor

Date

01-24-00 A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Ted A. Loxley

Serial No.: Group No.

Filed: Jan. 2000 Examiner:

For: Process and Apparatus for Cleaning Silicon Wafers

Commissioner of Patents and Trademarks

Washington, D.C. 20231

VERIFIED CERTIFICATION OF MAILING DATE (37 CFR 1.10(c))

I hereby certify that I have, in accordance with 37 CFR 1.10, deposited the papers or fees referred to below

- [x] new application transmittal and papers noted therein
- [ ] filing under 37 CFR 1.60 and papers noted therein
- [ ] file wrapper continuing application (FWC) 37 CFR 1.62 and papers noted therein
- [ ] other _____

and attached to this Verified Certification is a copy of these papers or fees identified above from the file of this application with the United States Postal Service on the date of January 22, 2000 in an envelope "Express Mail Post Office to Addressee" bearing Mailing Label Number EK216390975, as shown on the attached copy of the "Express Mail" Receipt.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Vincent A. Greene

(Typed or printed name of person making this verified statement)

Date January 22, 2000

Vincent A Greene

(Signature of person making this verified statement)

216390975

Process and Apparatus for Cleaning Silicon Wafers

This Application continues the disclosure of provisional application Serial No. 60/116,940 filed January 23,1999

The invention as shown and described herein relates to processes and apparatus for cleaning semiconductor wafers in the manufacture of microprocessors, integrated circuits, and other sophisticated electronic devices. The invention involves the discovery of a seemingly simple and very effective cleaning system that can remove or substantially eliminate sub 0.1 micron particles during the fabrication and processing of semiconductor wafers.

One preferred embodiment of the invention relates to a simple and unique cleaning apparatus comprising a special shaped receptacle designed for a single silicon wafer and having generally flat vertical walls parallel to the wafer that provide a narrow space for vertical flow of cleaning liquid. The cleaning is enhanced by charging the wafer to a relatively low voltage insufficient to damage the delicate circuitry.

The invention may seem simple in retrospect but is revolutionary in nature because it provides solutions to boundary layer problems that have mystified and plagued the semiconductor industry for decades. It involves a breakthrough in wet processing technology that should have tremendous value in the manufacture of the most advanced microchip devices.

INTRODUCTION

In the fabrication of microchips and other microelectronic devices the control of contamination is of utmost importance. As device geometries continue to shrink and die sizes grow, microcontaminants such as particles and metallic and organic impurities have an ever-increasing impact on device yields. Keeping wafer surfaces scrupulously clean throughout the wafer processing cycle is, therefore, an essential prerequisite to obtaining high yields in the fabrication of microelectronic devices.

Every wafer-processing step is a potential source of contamination. Only wet-chemical processing, or wet cleaning, between processing steps can reduce the number of particles on the surface of silicon wafers. Wet cleaning also removes metallic and organic contaminants as well as obstructive native-oxide films, which are not really a contaminant.

Wafer cleaning chemistry has remained essentially unchanged over the past 30 years, the most prevalent method in the industry still being hydrogen peroxide-based wet-chemical process - most notably the RCA Standard Clean, where wafers are immersed in several chemicals sequentially to remove particles, metallics, organics, and native oxides. The advent of smaller geometries and contamination-sensitive features forced the industry to seek new methods of wet chemical processing or more expensive alternatives.

Background of the Invention

The RCA Standard Clean developed by Werner Kern and other RCA scientists in the late 60's is extremely effective in removing contamination from silicon surfaces of semiconductor wafers and is today and has been the defacto industry standard for more than a quarter of a century.

The rapid progress in the semiconductor industry, due in large part to the effectiveness of RCA clean (i.e., SC1/SC2), is described in detail in Werner Kern's 1993 book "Handbook of Semiconductor Wafer Cleaning" (680 pages). This progress is also discussed in "Microchip Fabrication: A Practical Guide to Semiconductor Processing" (Second Edition, 1990) by Peter Van Zant.

Unless the context or logic suggests otherwise, the terminology, abbreviations and/or jargon employed herein is intended to have a meaning consistent with the usage set forth in these Kern and Van Zant books as would be understood by those skilled in semiconductor art.

The industry currently plans to reduce the circuit image size (also known as the line width or feature size) from 0.35 micron (um) to 0.25 micron. The leading industry group, SEMATECH, has set forth a detailed proposal for the 0.25 Micron Process which calls for around 360 process steps including more than 50 wet cleans. The detailed specifications (Steps 1 to 362) are set forth on pages B-3 to B-14 of the special printed SEMATECH publication, Technology Transfer No. 95042802-ENG. A large number of cleaning steps involve SC1, SC2 or other RCA

clean features, most or all of which could be modified in accordance with my invention to permit removal of extremely small or colloidal-size silica particles with a diameter of 0.05 to 0.1 micron or less which cannot be removed with current technology.

The 360-step wafer fabrication process described above involves only four basic operations. They are (1) layering, (2) patterning, (3) doping, and (4) heat treatments. A detailed overview of the wafer-fabrication process is set forth in Chapter 5 of the 1990 Van Zant book which is incorporated herein by reference. Pages 95 to 99 describe 11 basic steps employed in the formation of an MOS metal-gate transistor structure.

Cleaning steps 175, 212, 248, 284, and 320 of the aforesaid 362-step fabrication scheme shown on pages B-3 to B-14, described as Clean Post CMP, are critically important and pose a difficult problem. Megasonic cleaning devices are used to help remove microscopic particulate contaminants but have not been proven effective for particles with a particle size below 0.2 microns. The present invention provides the answer to this problem.

The industry currently plans to reduce the circuit image size (also known as the line width or feature size) from 0.35 micron (um) to 0.25 micron or less where a particle with a minute size, such as 0.03 to 0.05 micron, create serious problems and may be considered a "killer defect".

Prior to the invention, proposed improvements in wet cleaning and dry cleaning techniques offered no real hope of eliminating significant contamination by sub 0.1 micron silica particles. Therefore, killer defects were expected to prevent the semiconductor industry from achieving its optimistic defect goals for high volume manufacturing. The national SEMATECH roadmap has set forth model defect density (and, by inference, yield) requirements by technology generation. Table 1 is a portion of such roadmap related to defect density goals.

Table 1 Defect Goal Trends

DRAM equiv.	16 Mb		64 Mb		256 Mb		1 Gb	
Min. dimension	0.50 μm		0.35 μm		0.25 μm		0.18 μm	
Defects/cm² (%Yield)	0.1 (87%)		0.05 (90%)		0.03 (90%)		0.01 (95%)	
	# of defects	defect size	# of defects	defect size	# of defects	defect size	# of defects	defect size
Killer defects per 200 mm wafer*	28	0.10 μm	14	0.07 μm	9	0.05 μm	3	0.03 μm

In recent years chemical-mechanical planarization (CMP), makes it possible to employ smaller and smaller line widths which may approach 0.1 micron in the near future. Unfortunately CMP involves colloidal polishing that tends to promote excessive contamination with particles of aluminum oxide, silica and the like.

Summary of the Invention

The present invention relates to unique processes and apparatus for wet processing of semiconductor wafers in which the wafers are electrically charged and more particularly to a special wafer cleaning system that is effective in removing colloidal- or sub 0.1-micron size particles that cannot be removed effectively by any known prior-art process.

The RCA-type wafer cleaning methods that have been standard in the semiconductor industry for more than a quarter of a century have been improved substantially during the last decade by use of megasonic transducer means, mechanical scrubbers or other means that helps dislodge and remove the contaminating particles. Strong or violent agitation has been provided by rotating brushes, sonic energy beams, laser beams, water jets and/or other suitable impact means. Such wet-processing techniques have made possible effective removal of contaminants with a particle size less than 0.2 micron. Improved megasonic cleaning means can remove particles as small as 0.12 micron. However, wet cleaning techniques of the type mentioned above with the latest improvements are not expected to be effective in the future in removing sub 0.1-micron particles (e.g., those with a particle size below 0.07 micron).

Heretofore the semiconductor industry was convinced that wet cleaning methods would never be effective in removing adhered colloidal-size contaminant particles. The best

scientific minds grappling with the problem assumed, with good reason, that the tremendous van der Waals adhesive forces acting on colloidal-size particles at the wafer surface could not be overcome and that elimination of such particles by a simple wet cleaning operation was virtually impossible. The experts were convinced that the only real hope for success was a breakthrough in dry wafer cleaning technology, perhaps a sophisticated laser technique. A breakthrough or major discovery was considered essential if the industry was going to proceed with plans to reduce the feature size or minimum line width of the most advanced microchips to 0.15 micron or below.

The present invention provides the needed breakthrough and eliminates the need for a drastic switch from the usual wet cleaning systems to a unique dry system. It involves the amazing discovery that colloidal-size particles bonded to a wafer surface containing delicate microcircuits can easily be removed and repelled when the wafer is negatively charged in a suitable manner to a relatively small voltage, such as 2 to 60 volts, insufficient to damage vulnerable portions of the microcircuits or significantly reduce the yield of top-quality microchips.

The process and apparatus of the present invention are designed for use in the fabrication of microelectronic devices on semiconductor wafers where delicate microcircuits are formed on the front face of the wafer by 250 to 350 steps or more including many layering, patterning and doping operations and a large number of wet processing steps. The preferred process of

this invention is characterized in that the front face of each process wafer is provided with a negative electric charge of at least 0.4 volt during wet processing and an effective field intensity (e.g., at least 0.01 volts per millimeter) sufficient to dislodge and remove colloidal-size or sub 0.1-micron particles. The invention also contemplates reversing the charge on the wafer for specific applications.

The provision of an electric charge on each wafer in accordance with this invention is appropriate for batch-type wet processing operations in which 20 to 40 or more silicon wafers are treated simultaneously in one wafer carrier or cassette and also for operations where the wafers are treated one at a time. The invention is particularly well suited to water rinsing operations and to RCA-type wet cleaning operations including those with special modified sequences as mentioned in U. S. Patents Nos. 5,637,151 and 5,679,171.

In carrying out the electropurge wafer cleaning process of this invention, it may sometimes be advantageous to employ megasonic transducer means for directing sonic pressure waves in a direction generally parallel to the face of each wafer thereby enhancing particle removal. In some applications it may also be appropriate or desirable to provide means for rotating the wafer(s) during wet processing.

Maximum advantages of the present invention can be obtained when using the preferred embodiment wherein a single

wafer is subjected to wet processing in a flattened receptacle as in Figures 1 to 7 hereof. For example, a quartz glass receptacle, A, can be provided with a narrow internal cavity of a size to receive one 300 mm or 400 mm wafer having flat parallel glass walls spaced a short distance from the flat wafer faces. An aqueous solution or DI water would be caused to flow from the bottom to the top of the receptacle while the surface of the wafer was electrically charged. A desired negative charge is preferably induced by employing a positively charged metal plate, layer or coating at the flat outer surfaces of the receptacle as shown in Figures 6 and 7, for example.

One wet cleaning operation commonly involves RCA-type wet cleans with acid and alkaline treatments and a plurality of DI water rinses followed by spin drying or other final drying step. During all or most of the wet cleaning operations, the silicon wafer can be electrically charged in accordance with the present invention to a predetermined limited voltage, such as 2 to 60 volts. A substantially higher voltage may sometimes be tolerable, but charging the face of the wafer to a voltage of 100 volts or more is usually necessary or undesirable.

An excessive voltage is undesirable because of possible adverse effects on quality, uniformity and process yields and the increased risk of degrading the more delicate portions of the microcircuits.

In the semiconductor industry, one of the current target goals in microchip fabrication is to reduce the defect density to less than 0.03 defects per square centimeter (See Table 1). An object of the present invention is to reach that goal in a simple and effective manner by substantially eliminating "killer particles" and minimizing the number of troublesome particles (e.g., those with a particle size more than 10 percent of the minimum line width or feature size) which are highly undesirable.

The term "killer defect" is used herein in the broad sense to cover an unacceptable or intolerable defect in the microelectronic circuits of a semiconductor device or microchip caused by a contaminant particle trapped or embedded in the device during the fabrication process. A defect can be considered intolerable or unacceptable if it degrades the electronic circuits substantially or to such a degree that the electronic device has limited utility or is unacceptable to most customers.

The term "killer defect" is used in a narrow sense in Table 1 on page 5 of this specification to describe trapped or embedded particles with a particle size that is at least about 20 percent of the minimum line width or feature size (identified in the table as "Min. dimension"). That table from the SEMATECH roadmap indicates that one of the goals is to obtain a 90-percent yield of advanced (0.25 um) wafers with no more than 0.03 killer defects per square centimeter.

The term "killer defect", when used herein in the narrower sense, does not include colloidal-size particles with a size of 0.01 micron or less and does not cover very small microscopic particles (e.g., those with a particle size of from about 5 to about 10 percent of the minimum line width) that are highly undesirable and could affect the quality, reliability and useful life of the device.

Surface contamination is considered to be a major problem in the semiconductor, aerospace, and pharmaceutical industries. The adhesion of contaminants to silicon substrates is largely responsible for the yield loss in the manufacturing of VLSI and ULSI devices. Many methods for removing particles from silicon surfaces are currently used but the most common techniques are the wet chemical processes based on the hydrogen peroxide/ammonium hydroxide mixtures (SC1 or APM). The addition of megasonic energy during these processes has been proven to enhance particle removal.

Historically, SC-1 solutions were based on highly concentrated mixtures of ultrapure de-ionized water (DIW), ammonium hydroxide (NH_4OH), and hydrogen peroxide (H_2O_2), in a volume ratio of 5:1:1 (5 DIW : 1 H_2O_2 : 1 NH_4OH). Typically; wafers are immersed in these cleaning baths at 70-85°C for 10 minutes. Higher temperatures are not recommended in order to minimize thermal decomposition of hydrogen peroxide and evaporation of ammonium hydroxide. Wafer rinsing in DI water is usually conducted in intermediate and final steps.

During a SC-1 cleaning process, a cooperative and compensating action exists between the two chemical components. H_2O_2 oxidizes the silicon and forms a chemical oxide; the formation of this oxide is limited by the diffusion of the oxidizing species. Ammonium hydroxide, conversely, slowly

etches this chemically grown oxide. The result of these two processes is that a chemical oxide layer will continually be generated and removed. Particles are thus removed by this etching and undercutting action. Redeposition of particles onto the wafer surface is inhibited by the repulsion between the negatively charged silicon surface and the negative zeta potential that particles have in a SC-1 solution. Particle removal efficiency can be increased by increasing the etch rate of SiO_2. The etch rate, in turn, can be increased by using greater concentrations of NH_4OH or by elevating the process temperature.

The continually increasing integration of advanced IC manufacturing requires tighter process control and specifications. In addition, more stringent environmental requirements are being mandated to reduce chemical and water consumption and waste. The use of megasonic energy has been applied to many wafer surface cleaning procedures as a means to enhance particle removal, reduce chemical concentrations, and shorten process times. The acoustic waves needed for for cleaning are about 0.7 to 1.5MHz and are generated from piezoelectric transducers. When megasonics is used in conjunction with SC-1 solutions, particles of sizes 0.12 um or larger can be removed from the wafer surface.

The RCA Standard Clean, developed by W. Kern and D. Puotinen in 1965 and disclosed in 1970 [1] is extremely effective at removing contamination from silicon surfaces and

is the defacto industry standard [2]. The RCA clean consists of two sequential steps: the Standard Clean 1 (SC-1) followed by the Standard Clean 2 (SC-2). The SC-1 solution, consisting of a mixture of ammonium-hydroxide, hydrogen-peroxide, and water, is the most efficient particle removing agent found to date. This mixture is also referred to as the Ammonium-Hydroxide/Hydrogen-Peroxide Mixture (APM). In the past, SC-1 solutions had the tendency to deposit metals on the surface of the wafers, and consequently treatment with the SC-2 mixture was necessary to remove metals. Ultraclean chemicals minimize the need for SC-2 processing. SC-1 solutions facilitate particle removal by etching the wafer underneath the particles; thereby loosening the particles, so that mechanical forces can readily remove the particles from the wafer surface. The ammonium hydroxide in the solution steadily etches silicon dioxide at the boundary between the oxide and the aqueous solution (i.e., the wafer surface). The hydrogen peroxide in SC-1 serves to protect the surface from attack by OH by re-growing a protective oxide directly on the silicon surface (i.e., at the silicon/oxide interface).

Wafer rinse stages are an integral part of the chemical processes necessary in semiconductor device manufacturing. As an important stage in an integrated process, rinsing plays a central role in device yield, cost of ownership and environmental issues which continue to have increasing importance for the semiconductor industry. Because of these

considerations, there are significant benefits to developing optimized rinsing processes, including better device performance, reduced water consumption, shorter cycle times, higher tool utilization and higher throughputs - all leading to lower cost of ownership. The surface cleanliness of a wafer after a particular chemical process, may often be determined by the rinsing step. Contamination of a wafer surface by submicron-size particles, trace amounts of adsorbed metals and organic contamination, and carryover from the previous process stage all have significant effects on device yield and reliability. The rinse stage must preserve the results of previous chemical processing, remove specific carryover from the previous chemical treatment and maintain or improve surface cleanliness. In the coming years, as device densities increase and gate oxide thickness decrease, the effects of atomic-scale to sub micron-scale contamination on device degradation will become even more important.

Environmental and economic considerations are now significant when discussing rinsing processes. For example, in the front end of line (FEOL), through the first contact cut, approximately 20 separate cleaning sequences are needed to provide sufficient surface quality and to isolate each step from the others. A typical sequence may include, 4 cleaning baths, 4 rinses, and a drying step. For 20 FEOL cleans this is 80 rinses. Given the number of rinses and current

deionized water (DIW) use, this is 1,000 liters of DIW per wafer, just for FEOL. If we also consider back end of line (BEOL) and losses in the deionization system, over 3,700 liters of incoming water per wafer is required to meet current needs. With 5,000 wafer starts per week, this is 70 million liters of incoming water per month, just for rinsing.

Hydrofluoric Acid Solutions. Mixtures of concentrated hydrofluoric acid (49 wt% HF) and DI water have been widely used for removal by etching of silicon dioxide (SiO_2) films and silicate glasses (e.g., phosphosilicates, borophosphosilicates) that were grown or vapor deposited on semiconductor substrate wafers. The chemical dissolution reactions have been identified and described in the literature.

The thin layer of native oxide on silicon, typically 1.0 to 1.5 μm thick, is removed by a brief immersion of the wafers in diluted (typically 1:50 or 1:100) ultrapure filtered HF solution at room temperature.

Mixtures of hydrofluoric acid and ammonium fluoride (NH_4F) are known as buffered oxide etch (BHF) and are used for pattern delineation etching of dielectric films to avoid loss of the photoresist polymer pattern that would not withstand the strongly acidic HF solution without a buffering agent. Whereas the free acid is the major etching species in aqueous HF solutions, the ionized fluoride associate HF_2 is the major etchant species in buffered HF solutions.

Sulfuric-Acid/Hydrogen-Peroxide Mixtures. Removal of heavy organic materials from silicon wafers, such as photoresist patterns and other visible gross contaminants of organic nature, can be accomplished with mixtures of 98% H_2SO_4 and 30% H_2O_2. Volume ratios of 2 - 4:1 are used at temperatures of 100°C and above. A treatment of 10 - 15 min at 130°C is most effective, followed by vigorous DI water rinsing to eliminate all of the viscous liquid. Organics are removed by wet-chemical oxidation, but inorganic contaminants, such as metals, are not desorbed. These mixtures, are also known as "piranha etch" (because of their voracious ability to eradicate organics). Finally, it is advantageous after the rinsing to strip the impurity-containing oxide film on silicon or on the thermal SiO_2 layer by dipping the wafers for 15 sec in 1% HF-H_2O (1:50), followed by a DI water rinse.

Conventional RCA-Type Hydrogen Peroxide Mixtures.

These are the most widely used and best established cleaning solutions for silicon wafers. They are made up of ultra-filtered, high-purity DI water, high-purity "not stabilized" hydrogen peroxide, and either electronic-grade ammonium hydroxide or electronic-grade hydrochloric acid. The hydrogen peroxide must be very low in aluminum and stabilizer additives (sodium phosphate, sodium stannate, or amino derivatives) to prevent wafer recontamination. These mixtures, used in two process steps, have become known as RCA standard cleans (SC-1 and SC-2). The treatment is usually preceded by the preliminary cleaning.

The first step uses a mixture (SC-1) of 5:1:1 vol. DI water, H_2O_2 (30%, "not stabilized"), and NH_4OH (29 w/w% as NH_3) at 70°C for 5 min. followed by quench and rinse with cold ultra-filtered DI water. This deceptively simple procedure removes any remaining organics by oxidative dissolution. Many metal contaminants (group 1B, group 11B, Au, Ag, Cu, Ni, Cd, Co, and Cr) are dissolved, complexed, and removed from the surface.

The solution temperature should be 70°C for sufficient thermal activation, but must not exceed 80 °C to avoid excessively fast decomposition of the H_2O_2 and loss of NH_3. The treatment is terminated by, ideally, and overflow quench with cold DI water to displace the surface layer of the liquid and to reduce the temperature to prevent any drying of the wafer on withdrawal from the bath.

SC-1 slowly dissolves the thin native oxide layer on silicon and forms a new one by oxidation of the surface. This oxide regeneration has a self-cleaning effect and aids the removal of particles by dislodging them. These effects account undoubtedly for some of the beneficial results achieved by the treatment.

SC-1 also etches silicon at a very low rate. The standard 5:1:1 composition can have a surface roughening effect due to non-uniform local micro-etching. Lower fractions of NH_4OH have been proposed to avoid micro-roughening of the silicon, as further discussed in Sec. 4.4.of the Kern handbook.

The second step in the conventional RCA cleaning procedure uses a mixture (SC-2) consisting of 6:1:1 vol. DI water, H_2O_2 (30%, "not stabilized"), and HCl (37 w/w%). A solution temperature of 70°C for 5-10 minutes is used followed by quenching and rinsing as in the SC-1 treatment. SC-2 removes alkali ions, NH_4OH-insoluble hydroxides such as $Al(OH)_3$, $Mg(OH)_2$, and any residual trace metals (such as Cu and Au) that were not completely desorbed by SC-1.

SC-2 does not etch oxide or silicon, and does not have the beneficial surfactant activity of SC-1. Redeposited particles are, therefore, not removed by this mixture. The exact composition of SC-2 is much less critical than that of SC-1. The solution has better thermal stability than SC-1, and thus the treatment temperature need not be controlled as closely.

An optional etching step with dilute HF solution can be used between the SC-1 and SC-2 treatments of bare silicon wafers. Since the hydrous oxide film from the SC-1 treatment may entrap trace impurities, its removal before the SC-2 step should be beneficial. A 15-second immersion in 1% HF-H_2O (1:50) solution is sufficient to remove this film.

Each of the chemical cleaning and rinsing operations described above using alkaline or acid solutions and pure water (e.g., using SC-1 or SC-2 solutions or the like in RCA-type sequences) can be enhanced by charging each semiconductor wafer to a predetermined limited voltage, such as 2 to 60 volts or more, in accordance with the invention as described hereinafter. Providing an adequate or ample electric charge on the wafer during wet

processing in a receptacle of the type shown in Figures 1 to 7, for example makes possible remarkably efficient removal of sub 0.1 micron contaminant particles.

Ultrasonics and megasonics are commonly used particles removal techniques for silicon wafer cleaning. In ultrasonic cleaning, sonic energy in the range of 20-40kHZ is applied to a liquid within which the wafers are immersed. The force required to remove a particle in a sonic field, in the absence of any cavitation is: $F_r = ma$ where m is the mass of the particle and $a = 4\pi^2 f^2 A_m$. A_m is the amplitude and f the frequency of the sonic vibration.

In most commercial megasonic cleaners, it is this force, combined with the force created by cavitation that is generally considered important in the removal of particles.

Future Needs

Particle removal in the sub 0.1 micron regime is a key requirement for advanced cleaning technologies and is essential when making modern microchips with a line width of 0.25 micron. Unfortunately megasonic cleaning technology is ineffective in removing silica particles of such small size.

The simple fact is that current wet cleaning technology does not provide the answer to the microcontamination problem and would not permit reduction in line widths to 0.13 micron or below, the industry goal.

The aforesaid 1993 Kern handbook confirms the inadequacy of wet cleaning technology and indicates that dry cleaning processes will have to be used in the future to obtain the ultrapurity needed for the next generation of microchips.

Excessive costs have always been a major problem in semiconductor manufacture. Wafer cleaning costs during manufacture of microchips are extremely high and can be justified only because of the critical need to obtain adequate process yields. As recently reported in "Business Week" (December 22, 1997), a single eight-inch wafer of Intel's tiny 233-Mhz Pentium MMX chips contains about 210 chips worth $125,000.

The March, 1995, issue of "Semi/Sematech News" reported that every single six-inch silicon wafer processed in a fab uses 2,275 gallons of deionized water, 20 pounds of chemicals, over 3000 cubic feet of gases, and 285 kilowatt hours of electrical power and produces 2,840 gallons of waste water, 25 pounds of sodium hydroxide and 7 pounds of hazardous waste.

The various factors that determine process yields are discussed in chapter 6 of the 1990 Van Zant textbook, and Figures 6.2, 6.6 and 6.8 on pages 107, 113 and 114 are particularly pertinent with respect to cum yield.

Frequent wet cleans are essential during wafer processing to achieve satisfactory yields. In the 362-step manufacturing process previously described, more than 50 wet cleans would be employed. Wet benches are commonly used for wet cleaning operations and may employ robotic means for automatically advancing silicon wafers 25 to 40 at a time from one station to the next. A wet-bench set up is illustrated, for example, on page 138 of Kern's 1993 handbook.

When using RCA standard cleans (SC-1 and SC-2), a typical wet bench includes 5 or 7 recirculation immersion tanks, such as the tank shown in Patent No. 5520205, in which liquid is continuously pumped into the bottom of the tank and caused to overflow. Liquid cleaning, rinsing and drying steps in a typical wafer processing sequence (MOS gate oxidation) are shown by cross hatching in Figure 3 (Kern page 281). A 5-tank wet bench could, for example, start with an HF-strip and DI rinse followed by SC-1, DI rinse, SC-2 and DI rinse. Megasonic cleaning means would typically be used in the SC-1 bath but could also be used in the SC-2 bath and/or the rinse baths. A 7-tank wet bench could include a final HF bath followed by another DI rinse.

Needless to say, very large amounts of deionized (DI) water are required for the typical cleaning system. The water is extremely pure with a typical resistivity of 18 mega ohms as in Figure 4.16. The DI water is usually dumped after use but can sometimes be cleaned and recirculated (See Figure 4.15).

A 5-tank or 7-tank wet bench of the type described above could, for example, be employed for each of the wet clean steps 2, 5, 23, 35, 37, 63, 68, 70 and 108 of the 362-step manufacturing process previously described. It will be understood that the semiconductor wafers being processed must be dried at the conclusion of each wet clean before the next dry process step. A spin rinse dryer is commonly used for this purpose.

The specific 362-step fabrication process of the SEMATECH publication, pages B-3 to B-14 (reproduced in my Disclosure Document No. EH869229364) includes the lithographic (patterning-doping) sequence of described steps 14-22 and seven other lithographic sequences 25-34, 72-81, 82-92, 110-118, 119-128, 135-143 and 144-153 that are basically the same as the sequence 14-22, except for added inspection steps 31, 87, 124 and 149. Note also that there are slight differences at the ion implantation steps 78, 79, 89 and 90. Two other lithographic sequences 41-51 and 178-187 are quite similar but omit the implant step (20) and include added etching steps 48, 49 and 185.

The aforesaid fabrication process also includes the previously described layering-patterning sequences 195-204 and 214-224 involving metal or oxide deposits, steps 195 and 214, and chemical-mechanical polishing, step 211. It also includes three sequences 233-242, 269-278 and 335-344 that are basically the same as the described sequence 195-204 and three sequences 247-260, 283-296 and 314-331 that are basically the same as the described sequence 211-224.

The 362-step fabrication process includes more than 50 wet cleaning or wet processing operations that can be modified and improved in accordance with my invention as by inducing a substantial electric charge in each silicon wafer. These include eleven RCA-type wet cleaning operations (such as described steps 2, 5 and 23) including steps 35, 37, 63, 68, 70, 108, 129 and 154; four HF cleans, steps 65, 93, 103 and 133; five post CMP cleans, (such as described step 212) including

steps 175, 248, 284 and 320; nine NMP cleans (such as described step 209) including steps 227, 245, 263, 281, 299, 317, 334 and 347; ten resist strip with NMP (such as described steps 204 and 224) including steps 242, 260, 278, 296, 331, 344, 356 and 362' and fourteen resist strip with H_2SO_4 (such as described steps 13 and 22) including steps 34, 51, 62, 81, 92, 105, 118, 128, 143, 153, 161 and 187.

Proposed Laser-boil Cleaning System

In recent years a hybrid laser cleaning system has been proposed for use in cleaning semiconductor wafers. In this system a wafer is wetted and covered with a water film. A laser beam directed against the liquid film causes violent localized boiling that helps remove particulate contamination. It has not been demonstrated that this laser-boiling system is substantially more effective than megasonic cleaning or that it is a practical and reliable solution to the problems caused by sub-0.1 micron particles (However, such a system can be effective when modified to incorporate electropurge cleaning as in other versions of my invention.

Planarization and Post CMP Cleaning

Successful mass production of the advanced microchips used in today's computers became possible because of the development of a number of planarization techniques used to offset the effects of varied wafer topography. The techniques of multilayer resist processing, planarization layers, reflow, and chemical-mechanical polishing (CMP) are collectively known as planarization techniques.

The planarization methods do not guarantee an absolutely flat wafer surface ideally suited for subsequent lithographic operations. The only process that provides a global planarization of an entire wafer face is CMP, the same basic process used to flatten and polish the wafers sliced from the silicon crystal after crystal growing. Unfortunately the abrasive material used for polishing (i.e., silica or aluminum oxide) creates a major particulate contamination problem.

In a typical CMP polishing operation the wafers are mounted upside down on a holder and rotated in the other direction as in the SpeedFam CMP-V system shown and described in "Semiconductor International", May 1993 (Figure 10.16 of the 1993 article is a picture). An alkaline slurry of silica (glass) or aluminum oxide suspended in a mild etchant, such as potassium or ammonium hydroxide, is caused to flow between the wafer and the polishing pad.

The alkaline slurry chemically grows a thin layer of silicon dioxide on the wafer surface. The buffing action of the pad mechanically removes the oxide in a continuous action. High points on the wafer surface are removed until an extremely flat surface is obtained. A flatness specification across a 300 mm wafer can be in the 1500 Angstrom range.

CMP is commonly used to flatten the profiles that build up in multimetal interconnection schemes. In this use, the process takes on the added challenges of removing oxides and metals. The harder metals may require particulate abrasives,

such as aluminum oxide, that are more effective than glass or silica particles. However, silica is favored probably because it has less tendency to polish away portions of the functioning circuit parts (See Patent No. 5,676,587).

The removal of particulate contaminants from semiconductor wafers during post CMP cleaning operations is a most difficult and perhaps the most important of all wet processing operations in the fabrication of advanced microchips.

At the present time mechanical wafer surface scrubbers are considered the most practical when particulate removal is critical as in post CMP processing. The scrubbers usually hold the wafer on a rotating vacuum chuck. While being firmly held, a rotating brush is brought in near contact with the rotating wafer while a stream of deionized water (often with a detergent) is directed onto the wafer surface. This creates a high-energy cleaning action at the wafer surface. The liquid is forced into a small space between the wafer surface and the brush ends where it achieves a high velocity, which improves the cleaning action.

Care is needed to reduce secondary contamination caused by unclean brushes and cleaning liquid. Also, the proper brush height above the wafer must be maintained to prevent scratching of the wafer surface. The mechanical scrubbers are typically designed as stand alone units with automatic wafer loading capabilities or are incorporated into other pieces of equipment as in the CMP-V system to clean the wafers automatically before subsequent processing operations.

Although the mechanical scrubbing technique has become standard in post CMP cleaning operations, sometimes with subsequent wet cleaning enhanced with megasonic transducers, these cleaning methods do not provide a satisfactory way to eliminate sub 0.1 micron particles or a solution to the "killer defect" problem.

In the semiconductor industry, aluminum has for decades been the metal of choice in microchips in spite of its inferior conductivity. Typical CMP polishing equipment used in today's fabrication plants employ colloidal silica as the abrasive polishing media. The CMP operations and associated wet cleaning methods must be modified as chip makers overhaul their manufacturing processes in the recent switch from aluminum to copper, a more difficult metal (See U. S. Patent No. 5,676,587, for example. The industry is now entering the copper age.

The recent transition from aluminum to copper is proceeding at a feverish pace due to the tremendous potential and involves very large capital investments by a number of U. S. Companies. The transition to copper-based microchips is being driven by the strong demand for smaller and faster devices that consume far less power and can be manufactured at much lower costs. Copper interconnects are considered the key to delivering all of these potential advantages and capabilities because they should permit the commercial manufacture of

microprocessors with minimum line widths or feature sizes of 0.18 micron or less, perhaps as low as 0.13 micron in the near future.

This year the demand for copper process tools has taken off as chip makers feverishly go ahead with copper pilot line development in spite of unknown roadblocks in copper process technology.

It is manifest that copper carries electrical signals much faster than aluminum and that its electrical conductivity is at least 65 percent greater than that of aluminum. However, because copper is such a difficult material to deal with, aluminum had been the metal of choice. No practical and satisfactory way had been found to mass produce commercially-acceptable copper-based microchips. The situation changed last year with the disclosure by IBM that it expected to proceed with manufacture of copper-based microprocessors in the near future.

The impending switch from aluminum to copper requires satisfactory solution of several critical problems. Contamination of a microprocessor's silicon surface by copper metal has been a major roadblock for many years and remains a challenge.

The use of special barrier layers made of tantalum or tantalum nitride, for example, and the deposit of copper by electroplating techniques may provide a satisfactory answer to the more serious problems and may create some new problems in the manufacture of the most advanced microchips.

The Next Generation

Since the 1950s the semiconductor industry has maintained a constant rate of product evolution. In general, there has been a new product generation every three years. Within each generation, the density of memory chips has increased four times and logic chips 2 to 3 times. Every two generations (six years), the feature size has decreased by a factor of 2 and chip area and package pin count have increased by a factor of 2.

Projecting the future is always difficult but there are identified end points for chip circuits as we now know them. The Semiconductor Industry Association (SIA) technology roadmap profiles development to the 0.10 μm feature size level by the year 2007. That size will require chip densities of 16G (billion) bytes for memory and 20MB (million) logic gates. Wafer diameters will grow to 200-400 mm and die sizes will be in the 1000-mm range (1.2 inches per side).

Reaching this level will require development of x-ray lithography, low-resistance metals, low-leakage contacts, and ultra-clean materials and processes. Planarization techniques will be strained as the number of metal interconnect levels climbs to 6 or 7. Perhaps the major challenge will be reliable, stable gate oxides in the 35-Å range. Below 35 Å, carriers can tunnel through the layer, causing leakage problems. These technical problems must be overcome in a manufacturing atmosphere that is becoming increasingly expensive and requiring more automation and extensive measurement and process control programs.

Limitations on Wet Cleaning Methods

The RCA wet wafer cleaning methods developed by Werner Kern and RCA scientists have been the defacto industry standard for about three decades. Mr. Kern is still one of the most respected experts in this field.

In his 1993 "Handbook of Semiconductor Wafer Cleaning" it is stated:

"Significant advances in the science and technology of particles have led to a better understanding of the forces of adhesion, the nature of submicron particles in liquids, and gases, and the mechanisms of transfer solid surfaces. The work published after 1984 . . . . has resulted in improved high-purity processing and effective removal of particles from wafer surfaces, especially by the extended application of megasonic techniques."

"Van der Waals forces are the primary universal force of adhesion between particles and a wafer surface. Electrostatic double layer forces, capillary forces, and chemical bonds can also contribute significant adhesive force under appropriate conditions."

For the last 30 years the most competent scientists have been convinced that the primary force binding a colloidal-size particle to a wafer surface is van der Waals attraction which is universal and dominating when separation distances between a particle and a surface are extremely small (e.g., below 5 namometers). The forces of attraction increase as the particle size decreases so that it appears virtually impossible

to overcome the van der Waals forces when the particle size is 0.01 micron or less.

On this basis foremost experts, such as Werner Kern, concluded that wet cleaning processes could not provide a satisfactory way to remove colloidal-size particles when manufacturing the most advanced microchips and that new dry methods would have to be developed.

Attempts were made to improve the effectiveness of wet wafer cleaning processes by causing violent agitation of the liquid as by providing concentrated bursts of energy from lasers or megasonic transducers or by providing continuous mechanical agitation by rotating scrub brushes. However, such methods were not expected to be adequate for removal of sub 0.05-micron particles. Heretofore, more sophisticated dry cleaning methods seemed to provide the only real hope for minimizing particulate contamination when manufacturing advanced microprocessors with a minimum feature size or line width of 0.15 micron or less.

The universally accepted theories of the best scientific minds have turned out to be major impediments to progress in the wafer cleaning field. The present invention demonstrates serious flaws in those theories, particularly with respect to the nature and importance of van der Waals forces. Prior to the invention, the semiconductor industry had no reason to suspect that simple electrical equipment could provide a tremendous improvement in the effectiveness of wet cleaning processes.

Definitions and Terminology

The language used in the present disclosure should present no problem to persons skilled in the art of which the present invention pertains. The language should be construed in a reasonable and logical manner consistent with the context and normal usage in the art. Generally the technical terms and jargon can be construed to be consistent with the language or terminology employed in the textbook "Microchip Fabrication" (3rd Edition, 1997) by Peter Van Zant.

For example the terms angstrom, wafer boat, capacitor, CMP, CVD, CUM yield, DI water, die, dopant, DRAM, feature size, integrated circuit, ion implantation, killer defect, layering, lithography, LSI, patterning, passivation, photoresist, quartz, RTP, rinse, ULSI, VLSI, wafer and yield are defined briefly in the Glossary (pages 587 to 605) of said textbook.

The term "feature size" or "line width" is used herein in the usual sense to indicate the **minimum** width of pattern openings or spaces in a microelectronic device or microchip.

The term "megasonic" is used herein to describe energy waves generated from piezoelectric transducers in the 750- to 1500-kilohertz (kHz) range.

The term "field intensity" indicates the strength of an electric field. An "effective field intensity" as used herein is at least 0.01 volts per millimeter.

The term "charge density" indicates the degree of charge or current-carrier concentration in a region (e.g., coulombs/cm^2).

The term "electrode" is used herein to describe a silicon plate or wafer or a similar metal or metal-coated plate or device that can be electrically charged and employed to induce or create an electrical charge in a process wafer in accordance with the present invention.

A DC power source or power supply can be a direct current generator or battery or other source, such as a transformer-rectifier-filter arrangement.

The terminology used in the patent claims hereof should be construed in a reasonable manner in the light of the description and common usage. Unless the context suggests otherwise the terms are intended to be broad in scope rather than to have an unnecessary limited meaning.

Unless the context or common sense shows otherwise parts or percentages are by weight rather than by volume.

Description of the Drawings

Figure 1 is a front elevational view on a reduced scale showing a unique wafer cleaning means A in the form of a flattened quartz glass receptacle 10 having a narrow internal cavity that receives a single semiconductor wafer W;

Figure 2 is a fragmentary elevational view on a larger scale with the flat front wall 2 of the receptacle omitted and a portion of the marginal tube being shown in section, the vertical flow of liquid from the tube 5 being shown by the arrows;

Figure 3 is an enlarged fragmentary sectional view of the inclined tube portion 6;

Figure 4 is an enlarged fragmentary sectional view of the marginal tube 5;

Figure 5 is a fragmentary top view of tube portion 6;

Figure 6 is an enlarged fragmentary sectional view taken on the line 6-6 of Figure 2;

Figure 7 is an enlarged fragmentary sectional view similar to Figure 4 but taken on the line 7-7 of Figure 2;

Figure 8 to 12 are schematic views illustrating modified forms of apparatus that could be employed in the practice of this invention;

Figure 8 is a schematic foreshortened vertical sectional view on an enlarged scale showing a modified form of split glass receptacle (20) which may be opened for insertion or removal of the wafer;

Figure 9 is a schematic side elevational view of the receptacle (20) on a reduced scale;

Figure 10 is an enlarged fragmentary vertical sectional view similar to Figure 8 showing a modified glass receptacle suitable for wet cleaning of flat panel displays and/or field emission displays and including electrical means for charging the panel or wafer;

Figure 11 is a side view of the receptacle of Figure 10 similar to Figure 9; and

Figure 12 is a schematic vertical sectional view showing another modified form of wafer cleaning apparatus.

Description of Preferred Embodiments

One of the preferred embodiments of the present invention is illustrated in Figures 1 to 7 and employs a flattened wafer holder and receptacle 10 designed to receive a single semiconductor wafer w. This embodiment and other embodiments of a similar nature using single-wafer receptacles or the like are believed well suited for modern fabrication systems, particularly those that employ silicon wafers with diameters of 200 mm or more. When smaller wafers are employed, it may be desirable to employ other embodiments of this invention wherein 20 to 40 or more wafers mounted on a wafer carrier or cassette are cleaned and rinsed while being electrically charged.

Such wet-batch cleaning apparatus or a single-wafer apparatus of the type shown in Figures 1 and 2 can be modified using sonic energy, laser energy, scrubbing means or other means which may be appropriate in some applications. Modified versions of the apparatus can, for example, include megasonic transducer means for directing sonic pressure waves in a direction generally parallel to the wafer face (e.g., see U. S. Patents Nos. 4,869,278; 4,998,549 and 5,037,481).

Figures 1 to 7 illustrate a preferred embodiment of the present invention wherein a wafer carrier formed of glass, silicon or other suitable material has a narrow internal cavity that receives a single silicon semiconductor wafer and has means for charging the wafer to a small voltage during wet processing operations. These figures provide a simple schematic illustration of apparatus particularly well suited for use in the

practice of the invention and are intended to facilitate a ready understanding of the invention and the various ways the apparatus can be used in a high-tech microchip fabrication plant, for example in a typical 300-plus step manufacturing process that involves 40 to 50 or more wet processing steps.

While these drawings are to some extent schematic and omit features which may be considered valuable or important, they include the basic elements needed for practice of the invention and are drawn substantially to scale to provide an example of a simple quartz glass receptacle that would be suitable for commercial use as is or with simple modifications but probably would be improved greatly before use by a large manufacturer.

As shown, a wafer carrier A is provided in the form of an open-top quartz glass receptacle with top surfaces 1 and a pair of identical parallel flat glass walls 2 and 3 preferably spaced apart a distance of several millimeters, usually at least twice the thickness of the silicon wafer. The front and rear glass walls have flat vertical surfaces at opposite sides that are welded to the flat surfaces of straight vertical side bars 4 of rectangular cross section.

A quartz glass tube assembly 5 of semihexagonal shape is welded to the lower margins of the plates 2 and 3 which have an identical semihexagonal shape. It will be understood, of course, that the assembly 5 and the plates 2 and 3 could be semicircular, if desired, to conform more closely to the shape

of the circular semiconductor wafer w. A modern wafer used for manufacture of advanced microchips can have a diameter of 200 to 400 millimeters.

The glass tube assembly 5 has two oppositely inclined straight portions 6 welded to a straight horizontal portion 7. The flat surface 13 of tube portion 6 is welded to the flat inclined bottom surfaces of the plates 2 and 3 at opposite sides of a row of regularly spaced vertical openings 12 that direct liquid vertically in the direction of the arrows b (Figure 3). The horizontal tube portion 7 has a similar flat upper surface welded to the flat horizontal bottom surfaces of plates 2 and 3 on opposite sides of a row of closely spaced vertical openings 14 as shown in Figure 4. The tube sections 6 and 7 can have the same cross section throughout the length of tube assembly 5 so as to provide an unobstructed passage for flow of liquid between the two side bars 4 and access to all of the multiplicity of openings 12 and 14.

The liquid pumped into the bottom inlet openings 15 of tube portion 7 as indicated by the arrows a is directed vertically from those openings at a multiplicity of regularly or closely spaced locations as indicated by a multiplicity of vertical arrows in Figure 2. The water or cleaning liquid can be pressurized by the pump P, as in the embodiment of Figures 8 and 9, and caused to flow rapidly from the openings 12 and 14 as water jets or separate vertical streams, but this is not essential. The tube assembly 5 is designed to provide substantially

uniform upward flow of liquid across the full diameter of the wafer so that laminar flow will occur and unwanted eddy currents will be minimized or substantially eliminated. This assures rapid removal of all chemicals when changing from an acid to an alkaline wash or vice versa or changing to a DI water rinse.

The glass receptacle A of Figures 1 and 2 is open at the top edge 1 to permit vertical movement of the wafer w into and out of the narrow internal cavity 16 defined by the flat glass walls 2 and 3 and the marginal members 4, 6 and 7 (The large top opening is unnecessary in the embodiment of Figures 8 and 9 because the receptacle is split in half). The top edge portion at 1 provides a weir for overflow of liquid and can be flat or serrated. If the liquid overflows into a tank it can be filtered and recirculated, if desired.

Means are provided for holding and supporting a single semiconductor wafer in a vertical position midway between and parallel to the glass walls 2 and 3. If desired such means can be designed to permit or facilitate rotation of the wafer during the cleaning operation. As shown such means comprises a plurality (e.g., 3 to 5 or more) of wafer guide means 8 and 9 welded to or adhered to the marginal means 4, 6 or 7 and having grooves 11 that received and substantially fit the rounded circumferential edge portion of the wafer w. Such grooves can be shaped to maintain each wafer in the desired vertical position and can permit rotation of the wafer as by water pressure, sonic energy or mechanical means (e.g., see U.S. Patents Nos. 5,286,657 and 5,698,038).

In the practice of the present invention electrically-conductive plates, layers or coatings are provided at or near the surface of the glass receptacle to permit charging of the wafers and thereby effect removal of submicron particles adhering to the wafer surface. If a metal coating is employed, it is preferably applied at the outer surface of the plate 2 or 3. However, a layer or coating of silicon metal could be employed at the inner surface. In fact the plates 2 and 3 could be formed of silicon metal to minimize the distance from the charged plate to the wafer surface, thereby increasing the field intensity at a given voltage.

As shown herein a flat conductive metal charge plate 10 is mounted on the flat outer face of each plate 2 and 3. The plate is circular and has a diameter at least equal to and not substantially less than that of the wafer w, but other shapes and sizes may be appropriate or acceptable (e.g., when the wafer is rotated.

In order to obtain the desired uniformity it is desirable to divide the charge plate 10 or other charging means into a large number of sections so that independent computer control of the electric charge can be provided for each section. As shown the plate 10 is divided into more than 50 square sections to permit such computerized control of the charge density at each section.

In one embodiment of my invention, purging or cleaning of a semiconductor wafer can be carried out using wet cleaning means B of the type shown in Figures 8 and 9 comprising a flattened wafer holder and receptacle 20 formed of high-purity quartz glass having parallel flat circular wall portions 21 and 22 of uniform thickness and integral bottom and top portions 23 and 24 suitably connected to bottom inlet and top outlet pipes 44 and 45. A pump P is provided to cause the desired upward flow of DI rinse water or an aqueous cleaning solution through the receptacle 20.

The receptacle 20 can be split to form two halves 20a and 20b that fit together to form an airtight or watertight seal at the vertical split line 38. Optionally the receptacle may be divided into upper and lower sections with a seal at a horizontal split line. Suitable means may be provided to clamp or hold the two halves of the receptacle together and to maintain the desired seal. For example, some type of releasable clamping or holding means 39 can be provided to hold the halves 20a and 20b together during the wet cleaning operation and perhaps during a subsequent spin drying operation. Optionally, a series of very small glass projections or spacers 50 or other suitable holding means can be provided to locate or hold the wafer 30 or to hold it in a fixed position.

The unique quartz glass receptacle 20 is shaped to provide a shallow flat circular cavity 25 of uniform width with very shallow portions 26 and 27 of narrow cross section and uniform width at the opposite faces 31 and 32 of the wafer. Optionally the receptacle can be formed in one piece or welded

to join opposite halves, but this would require a narrow slot or opening at the top to permit a wafer to be lowered into and raised out of the cavity 25. Robotic means could be provided to lower, raise, and/or hold the wafer during wet cleaning and drying.

The cavity 25 of the receptacle 20 is shaped to assure laminar flow of liquid over the flat front and rear surfaces 31 and 32 of the silicon wafer 30, whose circular marginal surface 33 is preferably rounded. The wafer may, of course, have a notch or flat portion at the margin to assure proper positioning during manufacture. The inlet and outlet portions 23 and 24 of the glass receptacle are provided with smooth curved surfaces 23a and 24a, respectively, shaped to assure laminar flow free of eddy currents or turbulence as the aqueous liquid flows into or out of the narrow cavity 25.

The cavity 25 is shown as being generally circular and can have a uniform horizontal width preferably from about 2 to about 5 times the thickness (or horizontal width) of the silicon wafer 30 (e.g., a conventional 200 mm or 300 mm wafer). As shown the cavity width may be 3 or 4 times the wafer thickness so that the narrow spaces 26 and 27 between the wafer surfaces 31 and 32 and the glass surfaces 21a and 22a have a width of only a few millimeters, typically about 2 to 4 millimeters. The thickness of the vertical wall portions 21 and 22 is usually from about 2 to about 5 mm.

The RCA clean system (SC-1 and SC-2, etc) is preferred when carrying out the process of my invention using the single-wafer glass receptacle. The efficiency in removing submicron particles can, of course, be improved by employing megasonic energy. For example, optional megasonic cleaning means can be provided with an array of piezoelectric transducers near the outer marginal portions of the wafer 30 (at 60, Figure 9). Such means is located to cause the sonic pressure waves to travel through the liquid (from location 60) in a direction parallel to the vertical wafer surface. The impact of these pressure waves on contaminating particles with a diameter greater than 0.1 micron may be sufficient to dislodge them, but is not effective to remove smaller particles. Megasonic cleaning means are disclosed, for example, in Verteq Patents Nos. 4,869,278; 4,998,549 and 5,037,481.

The wafer cleaning apparatus B of Figures 8 and 9 is designed to receive flat discs or wafers 30 of circular shape but could be modified as in Figure 11 for wet cleaning of rectangular discs or wafers with or without the use of megasonic energy (at 60). The wet cleaning process and apparatus of my invention was designed primarily for use during the manufacture of microchips from circular silicon wafers, but is also important for use during the manufacture of rectangular flat panel displays (FPDs) and field emission displays (FEDs). The majority of FPDs are the color-active matrix liquid-crystal displays (AMLCD) most often seen as laptop computer screens.

Both color and noncolor LCD displays are manufactured using microchip-fabrication technology comparable to that described herein. However, the microelectronic devices, transistors, etc. are formed on relatively large rectangular glass plates rather than on a silicon wafer. The typical glass plate of an FPD has a width of at least one foot (300 mm) and is a borosilicate glass. Unlike a silicon wafer, the glass plate (e.g., plate 30') is nonconductive and cannot readily be charged by induction like the silicon wafer 30 of Figure 1. For this reason it is desirable to employ apparatus of a type specially designed for cleaning the rectangular FPD plate as shown in Figure 10, for example.

The cleaning means B' of Figures 10 and 11 is generally equivalent to the apparatus B of Figures 1 and 2 (except for the location of the glass plate 30' against or almost in contact with the flat wall portion 21' of the quartz glass receptacle 20') and is used in the same way (e.g., with the RCA clean sequences).

As shown the cleaning means A comprises a flattened quartz glass receptacle 20' having flat wall portions 21' and 22' of uniform thickness and integral curved bottom and top portions connected to inlet and outlet pipes 44 and 45. The receptacle is formed in two (non-symmetrical) halves that fit together at the vertical split line 38' to form an air-tight or liquid-tight seal throughout the periphery of the narrow cavity 25'. The portion 27' of that cavity between wall portion 22'

and plate 30' has a horizontal width that is usually no more than 3 or 4 millimeters and may, for example, be the same as that of the cavity portion 27 of Figure 8 so as to function in the same way.

The shape of the two-piece glass receptacle 20' differs from that of receptacle 20 at the inlet and outlet ends 28' and 29'. In Figure 10, the upper and lower portions 34 and 35 of the front half (20c) of the receptacle containing wall portion 22' is preferably symmetrical with only a slight curvature. In the rear half containing wall portion 21', the upper and lower portions are also symmetrical (as in Figure 8) with a curvature (e.g., at 23') comparable to that of inlet and outlet portions 23 and 24, but the inner surface at the margin of glass plate 30' is shaped to fit the plate at its marginal edge. If desired the receptacle may be made to fit the flat narrow marginal faces of the glass plate (at 33'), thereby eliminating a marginal gap. However, as shown in Figure 10, there is a marginal gap that's substantially filled with a narrow marginal strip 41 of generally triangular cross section. The strip extends around the entire periphery of the glass plate 30' to promote laminar flow of liquid and minimize unwanted eddy currents or the like. It can be rigid or flexible and can be formed of silicon, glass or other suitable materials.

In carrying out the process of the present invention, a small precision robot can be employed to pick up a simple wafer 30 or a single FPD plate 30' and transfer it to a wet

cleaning means B or B'. After the wafer or glass plate is placed in and securely located in the open half of the quartz glass receptacle 20 or 20', the receptacle is closed and held closed by clamping means or the like at 39 until the RCA or other cleaning sequence (or rinse) is completed.

The liquid flow provided by a water pump P or in other manner by a spray technique or vapor condensation is toward the outlet end from the inlet. The wafer 30 for example, can be in a substantially vertical position or in an inclined or horizontal position provided the flow is toward the outlet. If desired, one or more receptacles 20 can be spun about a vertical or horizontal axis at any desired speed to provide a centrifugal force on the liquid at the wafer surface. The desired movement of the water or other liquid over the wafer surface may be obtained with or without a pump P. It will also be understood that the DI water in the final rinse may be displaced with isopropyl alcohol prior to spin drying or other final drying operation.

The apparatus B of Figures 8 and 9, for example, is inexpensive and well suited for laboratory research. Apparatus of this type designed for research and development work in the field of wafer cleaning happens to be convenient for use in research involving electricity. The glass receptacle 20, for example, can easily be provided with a silver coating or other conductive metal coating (e.g., at 47 and 48) as part of an electrical circuit. The simple circuit shown in Figure 10, for

example, can easily be employed with the wet cleaning apparatus B or B' to apply a positive or negative charge.

That circuit includes a battery means or DC power source D with lines 1 and 2 connected to the negative and positive terminals, respectively, and an on-off switch. The power source D can include means to adjust and measure the voltage or emf.

It has been discovered that inducing a charge in a silicon wafer, such as the wafer 30, by providing a limited voltage, such as 2 to 60 volts, at the metal plate 47 or 48, is effective to remove submicron particles from the wafer surface during microchip fabrication. A voltage insufficient to damage a modern microchip with a line width of 0.15 micron can be sufficient to provide efficient removal of "killer" particles in the sub 0.1 micron range which heretofore could not be removed satisfactorily by any known wet cleaning method.

The embodiment of Figure 12 includes a thin rectangular quartz glass tank, vessel or receptacle and a plurality of permanently-mounted oxide-coated silicon wafers that serve as positive electrodes on opposite sides of each semiconductor wafer lowered into the vessel. If the vessel is designed to receive 2, 3 or 5 silicon semiconductor wafers (30), then the required number of positive silicon electrodes would, of course, be 3, 4 and 6, respectively. It could be feasible to clean 10

or 20 semiconductor wafers at a time in a tank 5 or 10 times the size of the one shown (which is designed to receive only one such wafer).

In the apparatus of the embodiment of Figure 12, DI water or other liquid is pumped into the bottom of the vessel and allowed to overflow at a weir or exit to an outlet pipe (not shown). The system could be fully automated. A small precision robot would pick up a single semiconductor wafer from a 25-wafer cassette or wafer carrier and insert this one wafer into the liquid bath midway between and parallel to the two outer positive-electrode silicon wafers.

The outer silicon-wafer electrodes can be connected in a suitable manner to the positive side of a power supply. They would be carefully and gradually charged to a positive emf of say 2 to 30 volts while the semiconductor wafer being processed is charged inductively to a comparable negative emf.

It is preferable to employ silicon wafers as electrodes when they are immersed in the aqueous bath as shown. All of the silicon surfaces of such electrode wafers will be completely oxidized prior to use so that substantial electrolysis will not occur in the bath. In the case where exposed conductor surfaces exist as IC components, the electrode voltages may be controlled at a low enough level to preclude destructive electrolysis.

In the manufacture of microelectronic devices or the like by the 362-step fabrication process of the aforesaid SEMA-

TECH publication, pages B-3 to B-14, contamination by sub 0.1-micron "killer" particles can be minimized by charging each process wafer to a predetermined limited negative voltage such as 2 to 60 volts during the various wet cleaning or processing operations while the wafer is within the glass receptacle (10) of Figures 1 and 2. For example, such an electric charge can be applied to the wafer (w) during each of the necessary wet processing operations including the RCA-type wet cleans, such as steps 2, 5, 23, 129 and 154; HF cleans, such as steps 65, 93 and 133; post CMP cleans, such as steps 175, 212, 248 and 320; NMP cleans, such as steps 209, 227, 263, 299 and 347; resist strips with NMP, such as steps 204, 224, 278 and 356; and resist strips with H_2SO_4, such as steps 13, 22, 62, 105, 143, and 187.

In carrying out the preferred wafer cleaning process of the present invention as herein described, the front face of the flat semiconductor wafer is negatively charged to a limit voltage, such as 2 to 60 volts, insufficient to create a substantial risk of damage to any of the delicate microcircuits on that face. The negative charge on the wafer surface at that face is associated with a substantial charge density and an effective field intensity of at least 0.01 volts/mm sufficient to assure effective removal of contaminant colloidal-size and sub 0.05 micron particles that are bonded to or adhere to the wafer surface because of van der Waals forces and other bonding forces. A variety of bonds may be involved including covalent, coulombic, ionic, electrostatic, dipole-dipole and hydrogen bonds.

While the negative charge can be obtained by use of an electric circuit that connects the silicon wafer to the negative terminal of a battery or other DC power supply, it is often preferable to obtain the necessary charge by induction as by placing a positively charged conductor or electrode near the wafer as shown in the drawings. If the electrode is spaced 1 to 5 millimeters away from the wafer, an adequate field intensity can be obtained even with a relatively low voltage, such as 1 to 2 volts.

The repulsive force exerted on a colloidal-size particle bonded to the wafer surface at a certain point when the surface is electrically charged at that point is directly proportional to the field intensity at that point. When such electrical charge is induced by a charged electrode nearby the field intensity can easily be calculated. It is directly proportional to the voltage at the electrode, inversely proportional to the dielectric constant of the liquid filling the space between the electrode and the wafer surface, and inversely proportional to the distance between the electrode and said point on the wafer surface.

The dielectric constant, commonly identified as epsilon (ϵ), is more than 70 when the liquid is water and can be reduced to about 50 when chemicals, such as ammonium hydroxide, are added to the water (e.g., as in RCA SC-1).

Assuming that the electrode is a flat metal plate parallel to the front face F of the wafer, spaced 5 millimeters

from such face, and having a charge of 3 volts, that the wafer is submersed in an aqueous liquid cleaning solution having a dielectric constant of 50, and that the charge density is substantial, the field intensity at any point on said front face spaced 5 mm from the electrode would be 3 divided by 250 (50x5) or 0.012 volts per mm. Such field intensity at a point on the wafer surface containing a bonded sub 0.1-micron particle or a colloidal-size particle could be adequate and effective to dislodge and remove such a particle in the practice of the present invention.

In the fabrication of advanced microcircuits where the feature size or minimum line width is reduced below 0.15 micron, it is necessary to limit the voltage to avoid damage to the circuitry. However, a substantial voltage, perhaps from 20 to 60 volts or more, may be desirable and tolerable if applied gradually.

If the voltage applied to the wafer surface is in the range of 0.4 volt to 1.5 volts, for example, the distance from the wafer surface to the electrode may have to be less than 3 mm (e.g., in the range of 1 to 2 mm) in order to have a field intensity adequate for effective removal of colloidal-size particles.

The charge density at the wafer surface is preferably maintained substantially uniform and should, of course, be substantial and more than adequate to permit effective electro-purging of the wafer(s).

Reducing the distance from the electrode to the wafer surface results in an increase in the field intensity. Such a reduction is easily accomplished in the embodiment of Figure 8. If the distance is greater than 4 mm because of the need for a glass wall near the wafer surface, it may be desirable or preferable to provide a silicon-metal layer or coating on the inner liquid-engaging face of the quartz glass wall (e.g., wall 21 or 22). In this way the distance from the positively-charged metal layer (electrode) to the wafer surface can be reduced to 1 or 2 mm. It will be understood that the spacing between the positive electrode and the wafer surface can likewise be reduced to a few millimeters (e.g., 1 to 2 mm) in other embodiments of the invention in order to increase the field intensity.

In carrying out the electropurge process of the present invention, it is necessary to provide the surface of the wafer with the desired charge of at least 0.4 volt and an effective field intensity. It will be readily apparent to those skilled in the art from the present specification and the schematic drawings how such charge can be provided and what electrical means could be employed for that purpose. It will be understood that such details or specifics are not needed for an understanding of the invention, that substantial portions of the complete electrical system that might be desired are not and need not be described herein.

Colloid Chemistry - Electrostatic Double Layer Repulsion

Finely divided particles dispersed or suspended in liquid systems are called colloids. Colloids and other surfaces immersed in a liquid media, such as ultrapure deionized water, acquire electrical charges primarily because of ion adsorption by the surface or ionization of surface groups. The net effect is that charge exchange takes place between the particle surface and the liquid media. The charge buildup on the particle is compensated by a buildup of charge of the opposite sign in the adjacent liquid layers. The charge on the particle surface, surrounded by a sheath of charge of opposite sign, constitutes an **electrostatic double layer** as depicted in Figure 10 on page 171 of Kern's "Handbook of Semiconductor Wafer Cleaning Technology" (1993).

The compensating charge in the liquid surrounding the particle is divided into two regions: (1) and inner compact layer of adsorbed ions that adhere to the particle; and (2) an outer diffuse layer of ions. The boundary between these two regions is the shear plane. When the particle moves through the liquid or the liquid flows past the particle, the ions in the compact layer move with the particle, while the ions in the diffuse layers move in the liquid.

The electric potential, assumed to be zero in the bulk liquid, has its maximum absolute value at the particle surface and decreases with distance perpendicular to the particle

surface, reaching zero at the outer boundary of the diffuse layer. The value of electric potential at the shear plane is called the zeta potential.

Zeta potential is important and the simplest potential of the colloid system to measure. By applying an electric field across a region of the liquid and measuring the resulting drift velocity of the colloid, the colloid mobility and potential (the zeta potential) can be determined. When measuring the zeta potential of silicon wafer surfaces, a streaming potential technique can be employed as described on page 172 of the aforesaid 1993 Kern handbook. Colloid surface charge, as opposed to the zeta potential, can be measured directly as indicated on that page.

Zeta potential generally depends on the ionic concentration of the liquid in which the surface is immersed, although the exact interaction is surface and ion specific. In aqueous systems, the zeta potential varies with pH as shown, for example, in Figure 11 on page 173 of Kern's handbook. Increasing the concentration of OH makes the zeta potential more negative, and vice versa.

Zeta Potential and Particle Deposition

While Figure 10, page 171 of Kern, illustrates the potential and charge distribution surrounding a spherical particle, the same description applies to a silicon wafer surface immersed in a liquid. It too is typically charged by the simple act of bath immersion. When the zeta potential of

the particle and the wafer are both negative, a repulsive force exists that creates a barrier to particle diffusion to the wafer surface.

A negatively charged colloidal particle is repelled from a negatively charged wafer surface by the charges adsorbed on the surfaces of each. If these repulsive forces dominate the interaction between the colloid particles and the surface, colloid deposition will not occur. This interaction is called electrostatic double layer repulsion (EDR).

Figure 14 on page 175 of Kern's handbook shows that colloid deposition on a hydrophilic wafer surface exhibits a dependence on pH very similar to zeta potential. At the pH of deionized water, silicon wafers and silicon particles exhibit negative zeta potentials and EDR effectively resists the deposition of the particles on the charged wafer surface. However, a small number of negative zeta-potential particles can deposit on the negative wafers. For example, it is known that such particles can deposit on the wafer from the water film that adheres to the wafer as it is withdrawn from the bath. For hydrophobic wafers, those prepared with an HF-last chemical clean, no adhering film remains during wafer withdrawal.

Because the deposit of particles on the wafer from the water film can be a significant problem, it is desirable to treat each wafer with isopropyl alcohol or other nonpolar organic compound (e.g., 1-methoxy-2-propanol or di-acetone alcohol before the wafer is dried (e.g., in a spin drier).

The effectiveness of EDR as a mechanism for shielding hydrophilic wafers and retarding colloid deposition becomes marginal if that zeta potential of the colloid is about -10 millivolts (Kern page 178).

It may often be preferable to apply a small negative charge to the wafer surface (e.g., up to 60 volts) during the acid cleaning step (e.g., when using hydrochloric or hydrofluoric acid as in DHF (dilute HF), HPM or an RCA-2-type wet clean). A megasonic transducer can be provided to supply sonic energy to assist in the electropurge cleaning. The megasonic assist can also be employed when the wafer is positively charged as described above. The use of megasonic transducers during RCA SC-1 and SC-2 cleans is standard practice today to assist in removing sub-micron particles but is not necessary when employing the electropurge process of the present invention.

It will be understood that the wet cleaning operations described above using a positive or negative charge on the wafer would preferably be carried out using a single-wafer receptacle, such as one of the general type shown in the drawings hereof, made of a suitable material, such as quartz glass or Teflon. The electric charge applied to the wafer surface being cleaned would be such as to provide an effective field intensity of at least 0.01 volts/mm and preferably at least 0.02 volts/mm.

As indicated on page 125 of the aforesaid Kern

handbook, typical RCA clean sequences include use of sulfuric acid (SPM) and hydrofluoric acid before the SC-1 and SC-2 cleans. Original RCA standard cleans employed substantial amounts of ammonium hydroxide and hydrochloric acid in the SC-1 and SC-2 recipes, more than necessary. A typical recipe was 29%NH_4OH:30%H_2O_2:DI water (1:1:5) or 37%HCl:30%H_2O_2:DI water (1:1:5). More dilute RCA-type cleaning solutions were better suited for modern microchips and various modifications of the RCA sequences were proposed, as in U. S. Patent No. 5,679,171, for example.

As the feature size or line width of advanced microchips is reduced below 0.15 micron, the concentration of the wet cleaning solutions can be critical. It becomes important to obtain a clean and smooth or atomically flat silica wafer surface (e.g., with surface roughness values under 2 Angstroms). In order to avoid excessive etching and unacceptable surface roughness, dilution of the RCA-type cleaning solutions is necessary or desirable.

The progressive reduction of MOS transistor dimensions will soon require ultrathin gate oxides less than 30 Angstroms thick and low rms interface roughness (e.g., below 2 Angstroms). In order to minimize interfacial microroughness for 15- to 30-Angstrom gate oxides, the wet cleaning or wet etching solutions should be diluted with substantial amounts of DI water. For example, a solution of 49%HF:98%H_2SO_4:H_2O(1:0.5:30) has been found suitable for wet chemical etching of the sacrificial SiO_2

layer. In order to reduce the objectionable surface roughening effect of SC-1 solutions, a dilute solution can be used, such as $NH_4OH:H_2O_2:H_2O$(1:8:64). Improved results have been obtained with dilute RCA (SC-1 and SC-2) cleans with chemical ratios around 50:1 and with ultra-dilute RCA (SC-1 and SC-2) cleans with chemical ratios in excess of 300:1. For example, when cleaning with an ultra-dilute SC-1 assisted by megasonic energy from a transducer, the final concentration can be around 1:5:1000 ($NH_4OH:H_2O_2:H_2O$). Dilutions of 1:2:100 as commonly used in production, when increased by a factor of 10, can still yield the desired protective oxide.

When employing a dilute or ultra-dilute RCA SC-2 clean recipe for wet cleaning (e.g., after a dilute or ultra-dilute SC-1 clean), it is not necessary to employ hydrogen peroxide. The ultra-dilute RCA clean can employ a 1000:1 dilution of 37%HCl in water at 45°C, for example. Metal removal efficiency of this solution is very high with or without the assistance of megasonic energy, particularly when the dilute solution is employed in the electropurge process of this invention (e.g., with a wafer charge of 2 to 60 volts and a field intensity of at least 0.02 volts/mm).

In the practice of the present invention electropurge cleaning with limited wafer charges, such as 2 to 60 volts, can be effective with the dilute RCA and ultra-dilute RCA (SC-1 and SC-2 cleans with or without the assistance of megasonic energy.

The need for ultrathin gate oxides to improve MOS device performance imposes stringent requirements on the silicon/gate oxide interface roughness to satisfy yield criteria and provide device reliability. Interface roughness not only degrades device performance by reducing the channel mobility, but may also affect reliability and yield by introducing asperities which act as electrical punctures. Even if the oxide is conformal, an asperity is an electric weak point due to the field lines associated with that topography. Therefore, it is important to consider the various contributions to roughness during device fabrication and employ methods which tend to minimize problems, especially when using ultrathin gate oxides with a thickness in the range of 15 to 30 Angstroms.

Advanced microchips are becoming more delicate and increasingly vulnerable as the feature sizes and line widths are progressively reduced. At the same time the industry performance standards for microelectronic devices are increasing to satisfy the need for better and more reliable devices. It is becoming more difficult to obtain satisfactory yields of advanced microchips with the quality, reliability and longevity meeting those high standards and the demands of consumers.

As the feature size is reduced, there is an increase in the number or frequency of imperfections, defects and potential problems areas, such as the electric weak points referred to above. In order to meet the reliability and yield requirements and avoid known and unknown hazards, there is reason

to disapprove questionable or risky procedures which might be unsafe or detrimental.

For these and other reasons, the electric charge applied to the silicon wafers in the practice of this invention should be limited and may be relatively small (e.g., from 2 to 60 volts). Excessive voltage should be avoided to minimize the risk of harm or damage to the delicate or sensitive microcircuits. A voltage of 100 volts or more is usually unnecessary or disadvantageous and might be imprudent for the more highly advanced microchips because of the potential detrimental, degrading or undermining affects on the more vulnerable or sensitive portions of the delicate microcircuits.

In order to help in the removal of sub-micron particles from the wafer surface, the surface should be charged with an effective negative voltage of at least about one volt to provide an effective field intensity of at least about 0.01 volts/mm at said surface. Such field intensity is preferably at least 0.02 volts/mm and sufficient to cause effective removal of sub 0.1-micron particles but insufficient to create a substantial risk of adverse affects or harm to the more vulnerable portions of the microcircuits.

The use of low voltages in the range of 2 to 60 volts is prudent and often preferred, particularly during BEOL wet processing where there are more problems and difficulties and the risk of harm or loss due to excessive voltage is much greater. Such low voltages provide a higher degree of safety and can be

remarkably effective in dislodging, removing and repelling sub 0.05-micron and colloidal-size contaminant particles which cause "killer defects" in advanced microchips, such as those having feature sizes of from 0.10 to 0.15 micron. The present invention is a godsend to the semiconductor industry, which heretofore had no practical and effective way to eliminate "killer" particles of sub 0.1-micron size or to reach target defect-density goals, such as those set forth in TABLE 1 on page 5 hereof. That table describes the SEMATECH yield model and equipment defect goals based on the model for pilot line and high-volume manufacturing. The table is taken from a printed SEMATECH publication dated July 31, 1994 and entitled "Contamination-Free Manufacturing Handbook" (Identified as 94062428A-TR). That publication provides informationthat covers most, if not all, aspects of contamination control methodology for semiconductor equipment and processes and is a convenient reference book for use by engineers, equipment designers, and contamination reduction specialists.

That publication points out that random particles represent a substantial and significant portion of yield loss, especially in the back end (BEOL) of a process, and that any systematic defect-reduction program needs to establish defect goals and then drive to achieve them. The most widely used approach for determining defect goals has been to take particle per wafer pass(PWP) numbers for next generation design rules. However, as pointed out in the SEMATECH publication, this approach is inadequate because it does not indicate or consider which particle goals are the first-order drivers of yield improvement.

The publication includes a footnote below TABLE 1 that reads as follows:

> "Since killer defect density is derived from yield and different process levels having varying sensitivities, defect size is not precise (± 100%). However, this size is often used for PWP goals as if it were precise and therefore causes problems in setting realistic detection and reduction goals."

The more recent National Technology Roadmap for Semiconductors as published by Semiconductor Industry Association (SIA) was reproduced in SEMICONDUCTOR INTERNATIONAL (January 1998), pg 40 (and Table 1) of which is incorporated herein by reference for all purposes. The SIA Roadmap estimates process-specific defect densities for future 0.25-micron (um) to 0.05-micron devices (up to the year 2012) and proposes defect targets for future generations of devices based on 60% yield for initial production. The SIA Roadmap focuses on equipment and process-induced defects (PIDs) per square meter. Average PIDs for the 0.25-micron generation were based on a study of PIDs at SEMATECH member companies. Table 1 on page 40 of that publication presents worst-case PID budgets assuming that all process levels are at minimum device geometries.

It will be understood that the above description is by way of illustration rather than limitation and that variations and modifications of the specific processes and devices disclosed herein may be made without departing from the spirit of the invention.

I claim:

1. In the fabrication of microelectronic devices on silicon semiconductor wafers where delicate microcircuits are formed on the front face of a flat silicon wafer having a diameter of at least 200 mm by more than 200 steps including many layering, patterning and doping operations and at least 30 wet processing steps, characterized in that each semiconductor wafer is electrically charged from a direct current source during wet processing steps to provide an effective field intensity.

2. A process according to claim 1 characterized in that the field intensity at the wafer surface is sufficient to dislodge and remove sub 0.1 micron particles.

3. A process according to claim 1 wherein a wafer is charged to a voltage of from about 2 to about 60 volts during wet processing operations.

4. A process according to claim 1 wherein a wet processing operation includes chemical mechanical polishing with colloidal-size abrasive particles and subsequent chemical cleaning of each wafer to remove such particles while the wafer is charged to a voltage sufficient to dislodge and repel colloidal-size particles.

5. A wafer cleaning process according to claim 1 wherein a wet processing operation includes treatment of each wafer with a dilute high-purity acid solution while the wafer surface is electrically charged.

6. A process according to claim 1 wherein the wet processing operation includes treatment of each wafer by a non polar compound, such as isopropyl alcohol, 1-methoxy-2-propanol or di-acetone alcohol, before drying the wafer.

7. A process according to claim 1 wherein particulate contaminants are removed and substantially eliminated from a wafer by charging the wafer with a negative voltage of from about 2 to about 60 volts while providing a field intensity of at least 0.02 volts/mm at the wafer surface sufficient to dislodge, remove and repel substantially all of the harmful sub 0.1-micron particles.

8. A wet cleaning process wherein a semiconductor wafer is cleaned by thorough rinsing in DI water characterized in that the wafer is charged during rinsing to a voltage of at least 100 volts in such manner that colloidal-size and submicron killer particles bonded to the front face of the wafer containing the delicate microcircuits are effectively removed or eliminated.

9. A process for economical wet cleaning of semiconductor wafers during the fabrication of microelectronic devices wherein a single flat wafer is mounted in a fixed position in a narrow shaped receptacle having a flat wall portion parallel to the front face of the wafer and spaced therefrom a short distance, preferably less than 5 mm, and wherein a sequence of several wet cleaning operations is performed on said wafer while it is held in the desired position in said receptacle.

10. A process according to claim 9 wherein the semiconductor wafer is subjected to a series of RCA wet cleaning operations, and megasonic energy is directed generally to the front of said wafer during such operations.

11. A process according to claim 9 wherein an SC-1 cleaning operation is employed using a solution of water, hydrogen peroxide, and ammonium hydroxide including from about 10 to abut 30 percent by weight of an alcohol, such as ethyl alcohol or isopropyl alcohol.

12. A process according to claim 9 wherein at least one face of the semiconductor wafer is charged to a limited but effective voltage, such as 2 to 60 volts, during a wet cleaning operation in said receptacle.

13. A process according to claim 9 wherein a flat electrode with a diameter or width comparable to or larger than that of the semiconductor is provided at the outer face of the glass receptacle to induce the desired electrical charge at the wafer surface during wet cleaning.

14. A process according to claim 3 wherein the front face of one thin plate or wafer containing the delicate microelectronic devices is subjected to a series of wet cleaning steps while that plate is mounted in a fixed position in the internal cavity of a flattened quartz glass receptacle.

15. Apparatus of the character described for wet cleaning of wafers during the fabrication of microelectronic devices comprising a shaped receptacle having a cavity for

receiving at least one semiconductor wafer, means for admitting a liquid to said cavity, and means for charging said wafer with a limited voltage effective to facilitate removal of submicron particulates.

16. Apparatus according to claim 15 for wet cleaning of wafers during the fabrication of microelectronic devices comprising a shaped receptacle with a narrow cavity of a size to receive a single flat wafer, said receptacle having a flat wall portion parallel to the wafer and spaced from the wafer a distance of from about 1 to about 5 mm to cause uniform flow over the entire face of the wafer.

17. Apparatus according to claim 16 wherein a process wafer is mounted in said cavity and exterior means are provided to induce an electric charge of at least 2 volts in said wafer during wet cleaning.

18. A process of the character described for fabrication of microelectronic devices on silicon wafers wherein microcircuits are formed on the front face of a wafer by a plurality of layering, patterning, doping and heating operations and the wafer is wetted and repeatedly subjected to cleaning, rinsing and drying operations to remove contaminants, characterized in that said front face of the process wafer is artificially charged during wet processing with a negative voltage of at least 2 volts sufficient to facilitate removal of sub 0.1 micron contaminant particles bonded to the wafer surface during the wet cleaning operations.

19. A process according to claim 18 wherein the front face of the process wafer is subjected to wet CMP polishing with colloidal silica or alumina particles having an average particle size of from 0.01 to 0.03 microns and is thereafter subjected to chemical cleaning and DI rinsing operations while said front face is negatively charged to a voltage sufficient to cause efficient or substantially complete removal of sub 0.05-micron contaminant particles bonded to the wafer surface.

20. A process according to claim 1 for fabrication of microchips having a minimum line width or circuit image size less than 0.15 microns wherein the fron face of each wafer is subjected to the wet CMP polishing with colloidal silica or alumina particles and is thereafter subjected to a wet cleaning operation for 0.5 to 5 minutes while said front face is negatively charged to a substantial voltage, such as 10 to 40 volts or more, sufficient to remove colloidal or sub 0.05 - micron contaminant particles, the voltage and rate of large of the wafer surface being applied or controlled during said wet cleaning operation in such manner as to minimize or limit damage or alteration of the delicate microcircuitry.

21. In a process of the character described for forming delicate microcircuits on the front face of a semiconductor wafer wherein the wafer is subjected to a large number of layering, patterning and doping operations and many wet processing steps to remove organic, metallic and particulate contaminants, the improvement in which the front face of the wafer is provided with a limited electric charge of at least 2 volts during wet processing steps insufficient to degrade the microcircuits, the charge being sufficient to provide a field intensity at said front face effective to dislodge and remove sub 0.1-micron particles bonded at the wafer surface.

22. A process according to claim 20 wherein said field intensity is at least 0.02 volts/mm and sufficient to provide efficient removal of colloidal-size particles.

23. A process according to claim 22 wherein the front face of the wafer is charged to a voltage of from about 1 to about 60 volts.

24. A process according to claim 23 wherein a single silicon wafer with a diameter of at least about 200 mm having a front face with microcircuits having a feature size or line width less than 0.18 micron is wetted and cleaned by charging said front face to a voltage of from 2 to 60 volts, thereby causing colloidal-size particles to be dislodged, released and removed.

25. A process according to claim 24 wherein the front face of the wafer is charged to a field intensity of at least 0.02 volts/mm during washing of the wafer in a highly dilute alkaline solution.

26. In the manufacture of advanced microchips, a process for forming delicate microcircuits on the flat face of a semiconductor wafer in which the wafer is subjected to a large number of layering, patterning and doping operations and many wet cleaning steps with acid and alkaline solutions and pure water to remove intolerable contaminants, characterized in that the wafer face containing said microcircuits is electrically charged to a limited voltage of at least 2 volts to provide an effective field intensity that causes sub 0.1 micron particles bonded at the wafer face to be released and removed.

27. A process according to claim 26 wherein said wafer face is negatively charged to a voltage of from 2 to 60 volts sufficient to cause efficient removal of harmful particles with a particle size of from 0.01 to 0.1 micron.

28. A process according to claim 26 wherein said wafer face is provided with a limited electric charge of at least 10 volts during most of said wet cleaning steps to minimize particulate contamination.

29. In the manufacture of advanced microchips from flat semiconductor wafers having delicate microcircuits formed on one face, an RCA-type wet cleaning process wherein a single wafer is treated in an aqueous alkaline solution containing hydrogen peroxide and thereafter treated in an acidic solution, rinsed in pure water and dried, characterized in that the wafer surface containing said delicate microcircuits is electrically charged during the wet cleaning process to cause effective removal of sub 0.05-micron particles that are strongly bonded to the wafer face.

30. A wafer cleaning process according to claim 29 wherein megasonic energy is employed to assist in the removal of the contaminating particles during the treatment in the alkaline solution and said wafer surface is charged to a negative voltage of from 2 to 60 volts during the cleaning and rinsing steps.

Abstract of the Invention

An effective electropurge process and apparatus for wet processing of semiconductor wafers applies electrical charges to the wafer surface with an ample voltage sufficient to provide an effective field intensity which can substantially eliminate intolerable sub-0.05 micron "killer" defects when making highly advanced microchips with a feature size or line width less than 0.15 micron. The process can be used for automated wet-batch cleaning operations using cassettes that hold 10 to 50 wafers at a time and in various other operations involving megasonic transducers, mechanical brush scrubbers, laser cleaners and CMP equipment. The electropurge process is primarily intended for Fab plants where large wafers with a diameter up to 400 mm require 250 to 350 steps including many dry layering, patterning and doping operations and at least 30 wet processing steps.

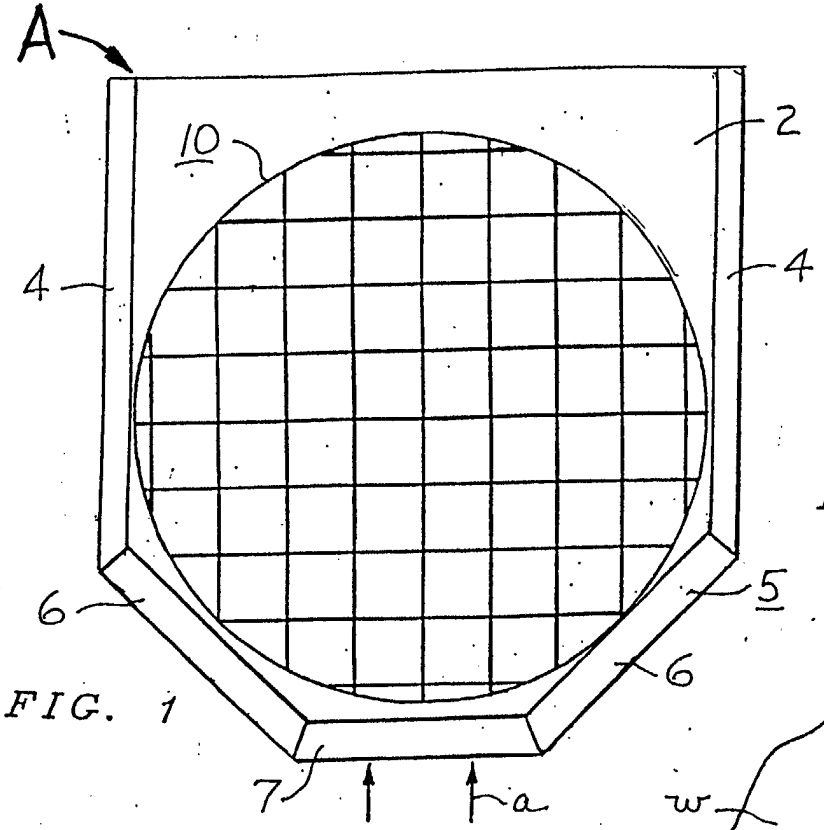

FIG. 1

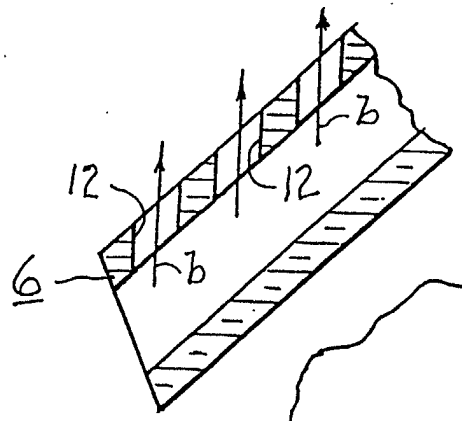

FIG. 3

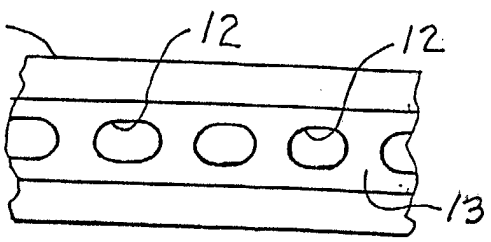

FIG. 5

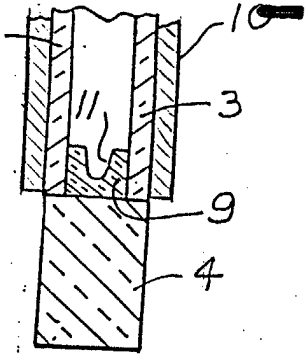

FIG. 6

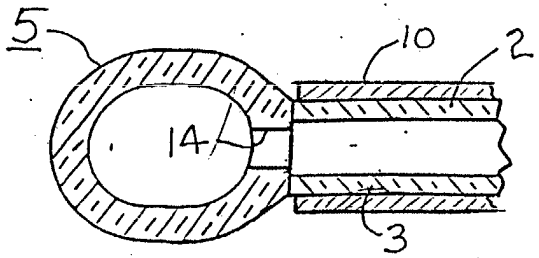

FIG. 4

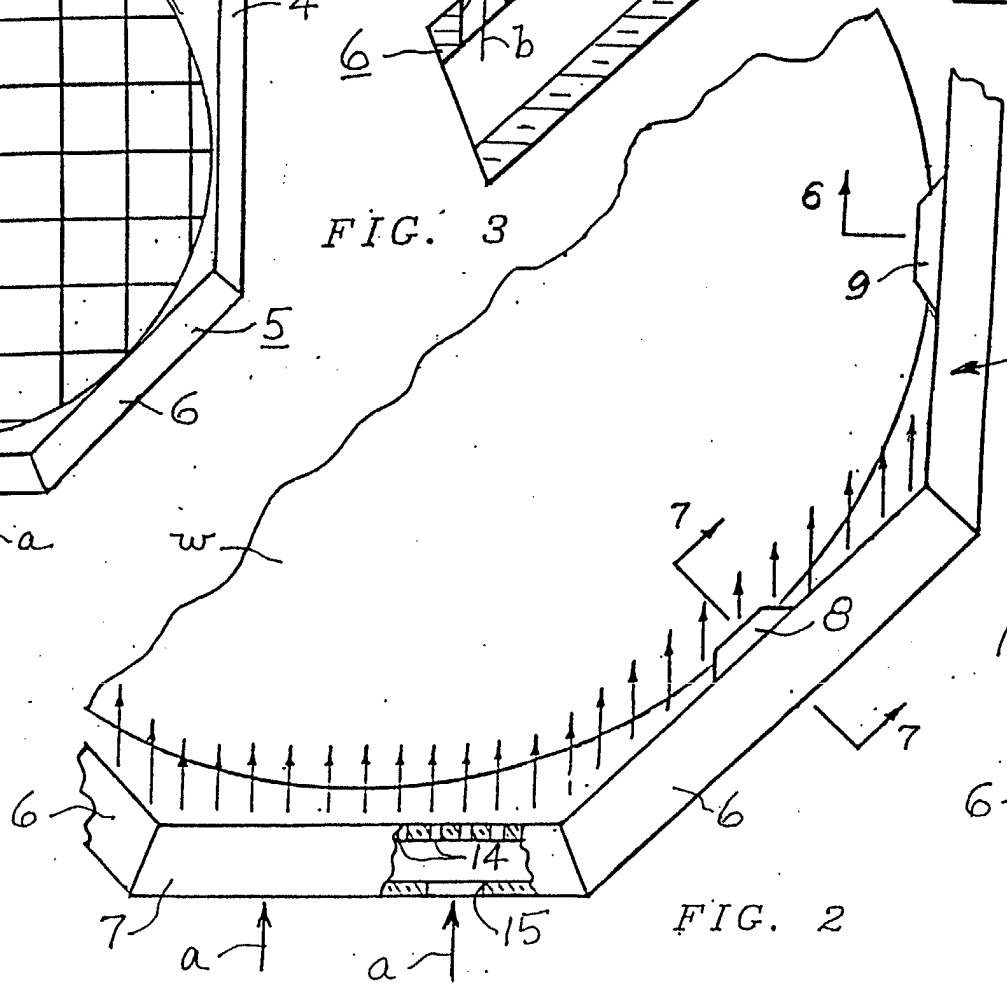

FIG. 2

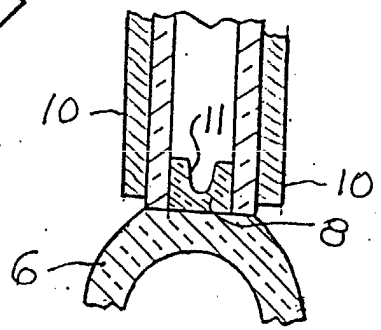

FIG. 7

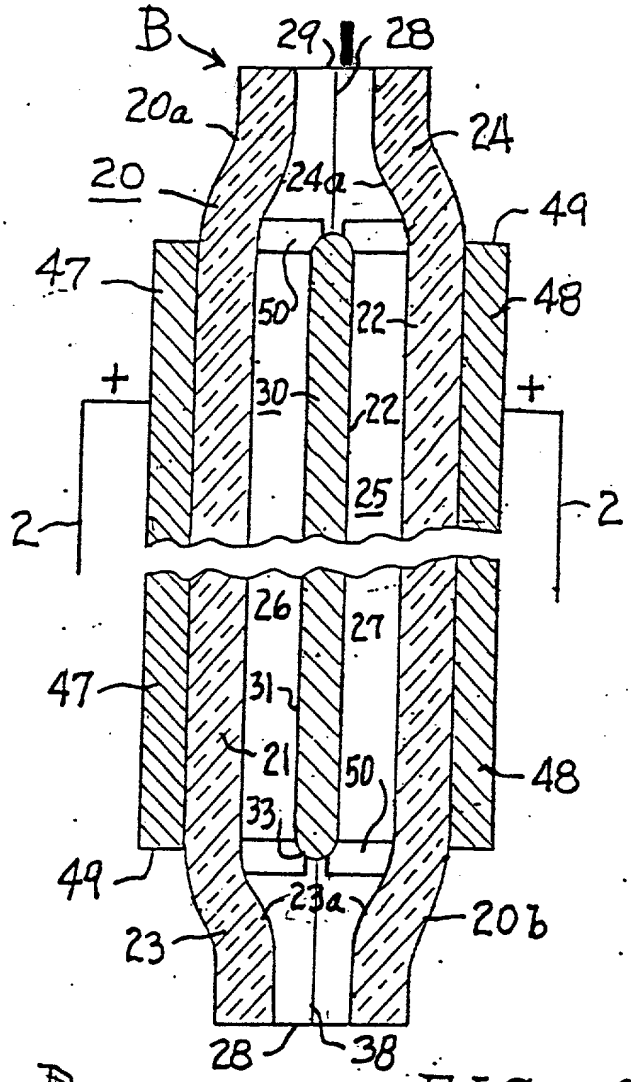

FIG. 8

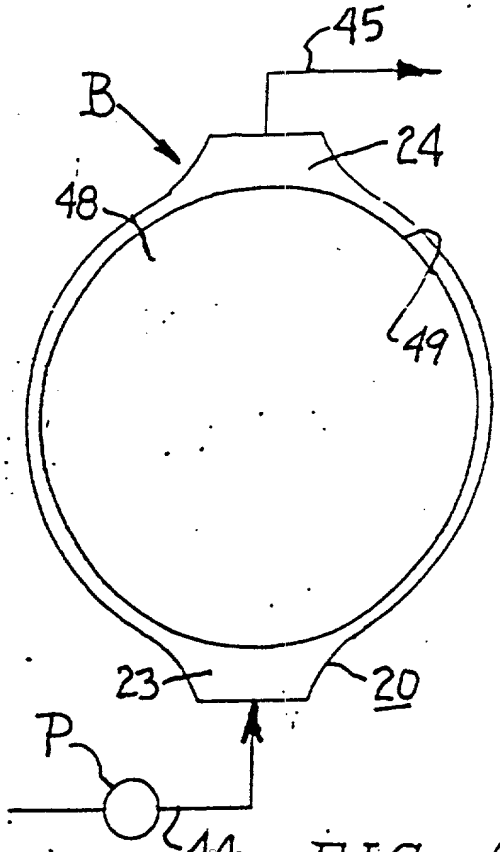

FIG. 9

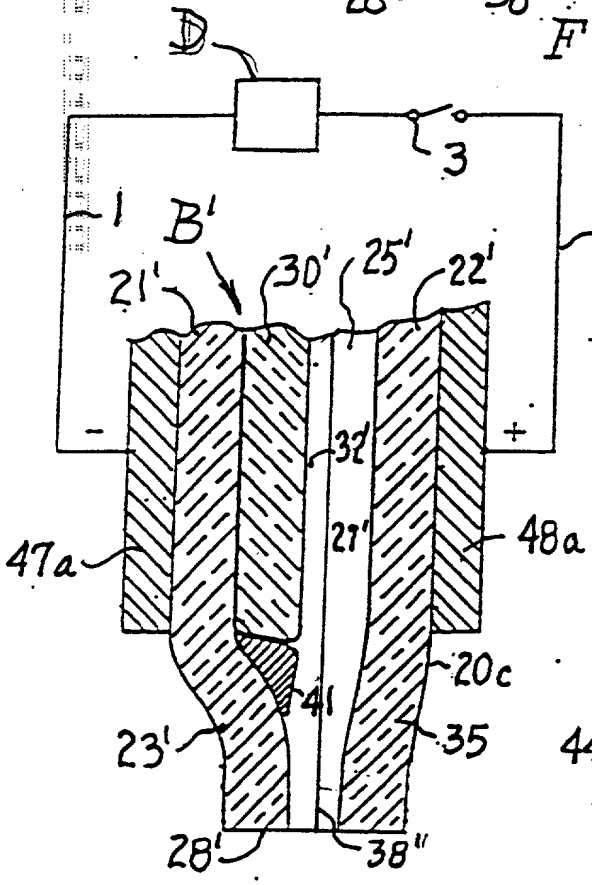

FIG. 10

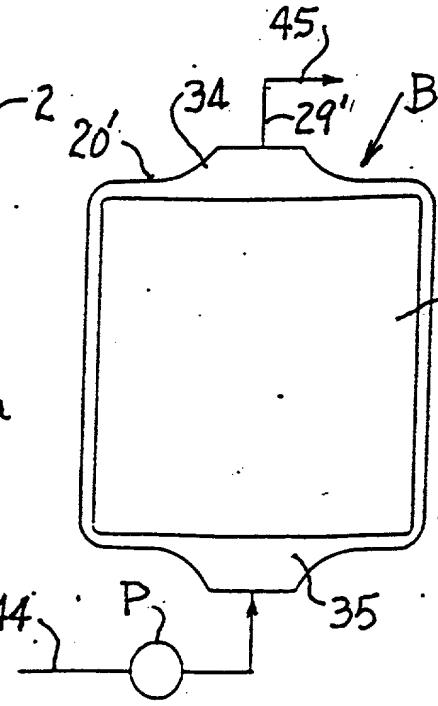

FIG. 11

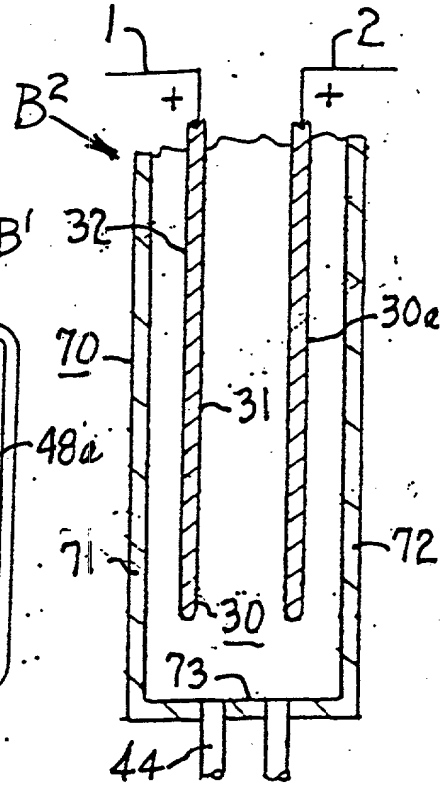

FIG. 12

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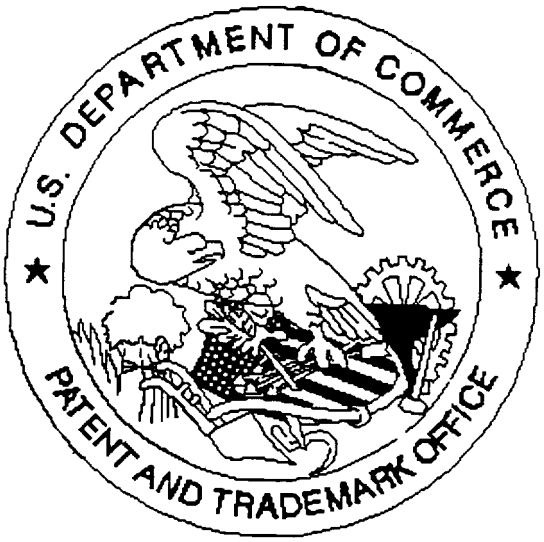

SCANNED 2

Application deficiencies were found during scanning:

☐ Page(s) 2 of 7 - 7/7 of Declaration were not present for scanning.
(Document title)

☐ Page(s)_____ of _____ were not present for scanning.
(Document title)

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